


PAGE	TITLE
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[illegible]

			
Title			
<b>COVER SHEET</b>			
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	4.02	
Date:	Thursday, July 03, 2014	Sheet	1 of 35

## Component value change history

4 Layer, 4mil 50ohm +/- 15% X

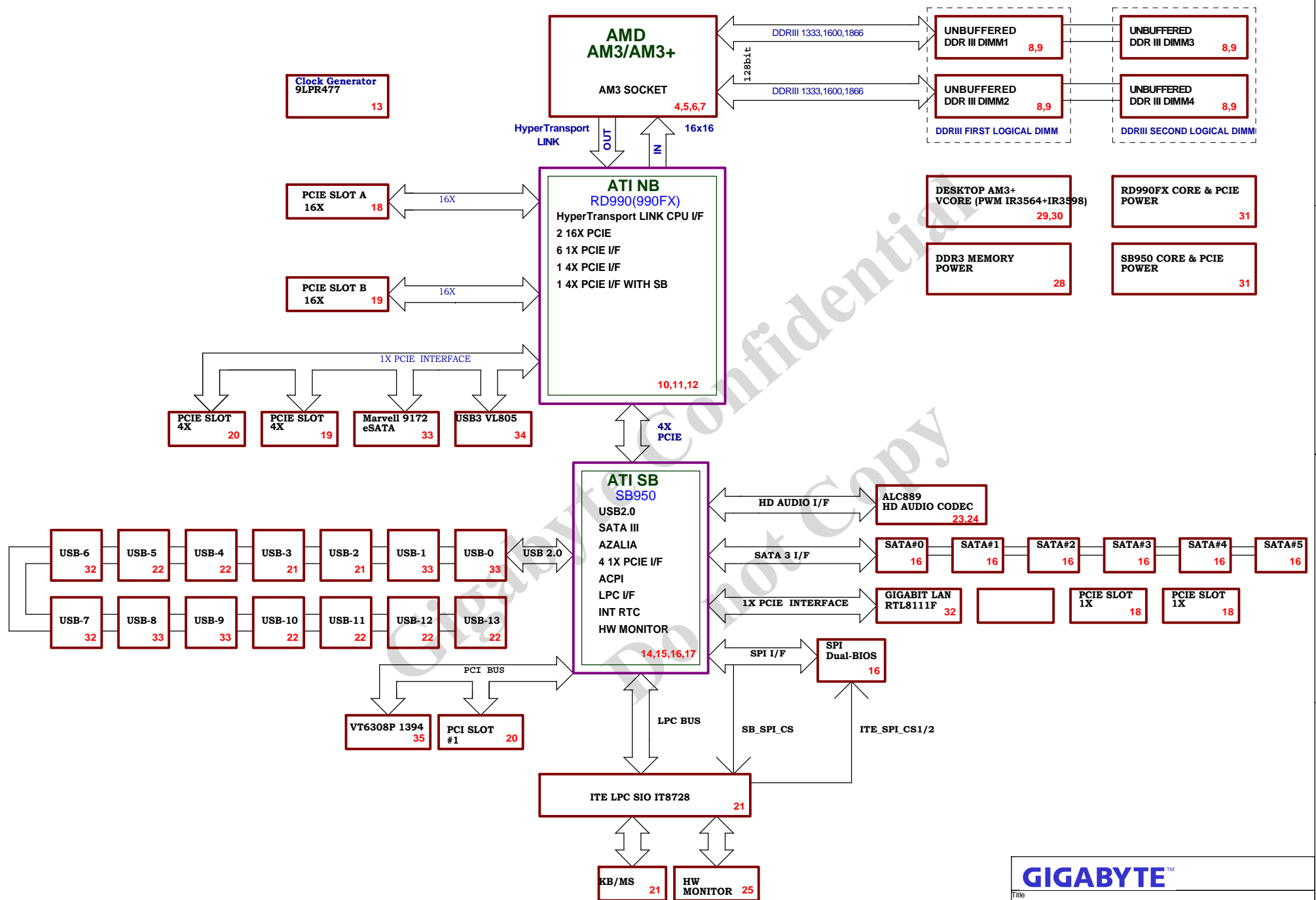
**Version: 4.02**

**P-Code:**  
**U98145-0**

[illegible]

**Circuit or PCB layout change for next version**

[illegible]



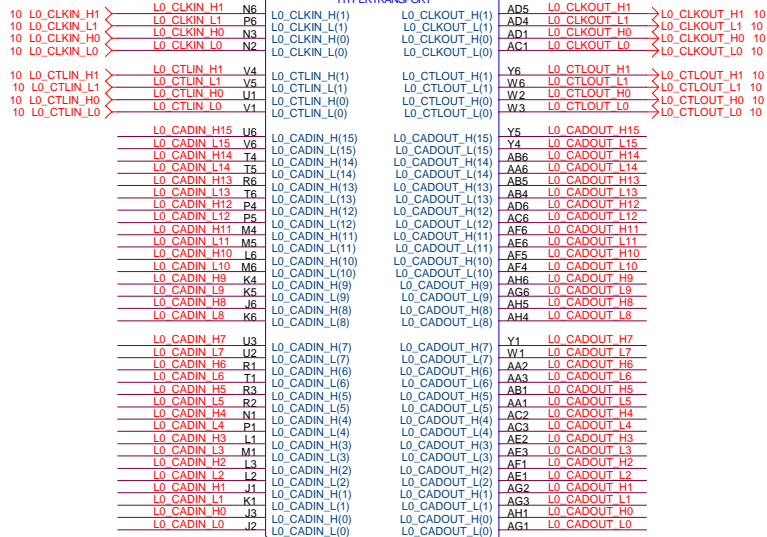
GIGABYTE™

BLOCK DIAGRAM			
Title	BLOCK DIAGRAM		
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	4.02	
Date:	Thursday, July 03, 2014	Sheet	3 of 35

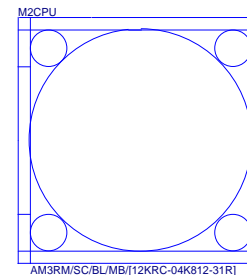
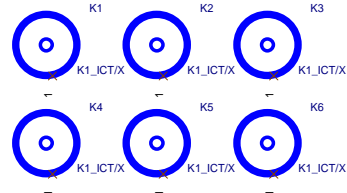
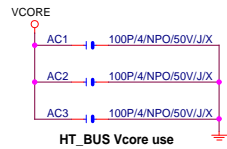
L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] 10  
 L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] 10  
 L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] 10  
 L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] 10

M2CPUA

HYPERTRANSPORT

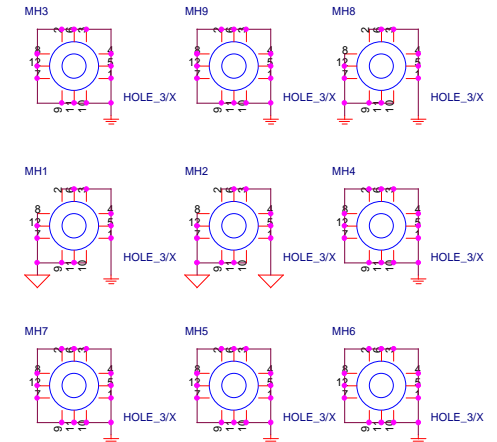


CPU-SK/941AM3/S/GF/[10SC1-A01942-01R\_10SC1-A01942-02R]

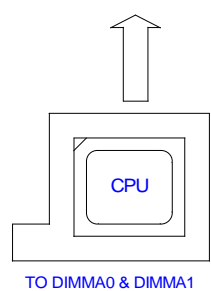
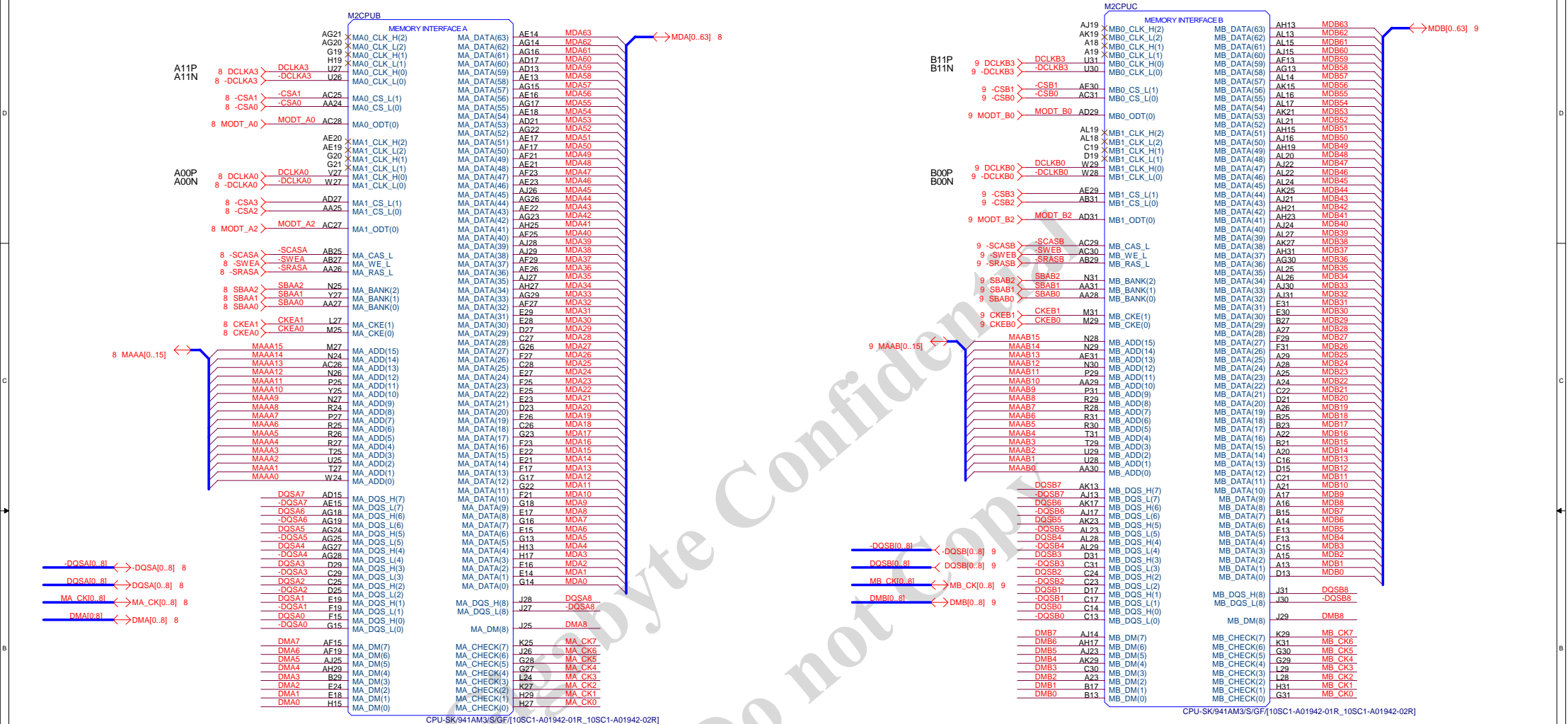


CPU\_VDD\_RUN = VCORE  
 CPU\_VDDA\_RUN = VDDA25  
 VLDT\_RUN = VCC12\_HT  
 CPU\_VDDIO\_SUS = DDR15V  
 CPU\_VDDR = CPU\_VDDR12

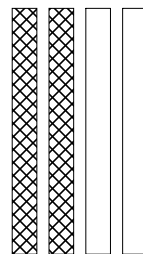
VLDT\_A = VCC12\_HT  
 VLDT\_B = HT12B



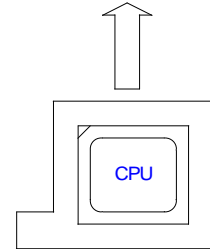
<b>GIGABYTE</b>		
Title		
<b>COVER SHEET</b>		
Size	Document Number	Rev
Custm	<b>GA-990FXA-UD3</b>	<b>4.02</b>
Date:	Thursday, July 03, 2014	Sheet 4 of 35



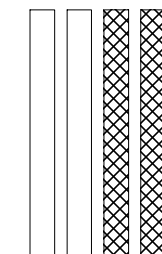
MEM CHA




A0 A1



MEM CHB

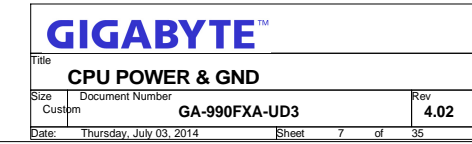
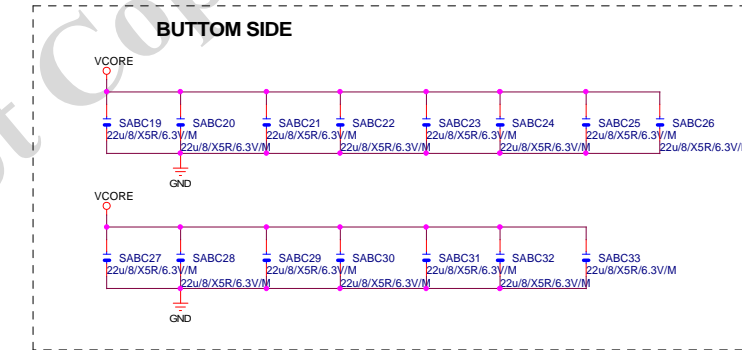
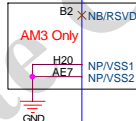


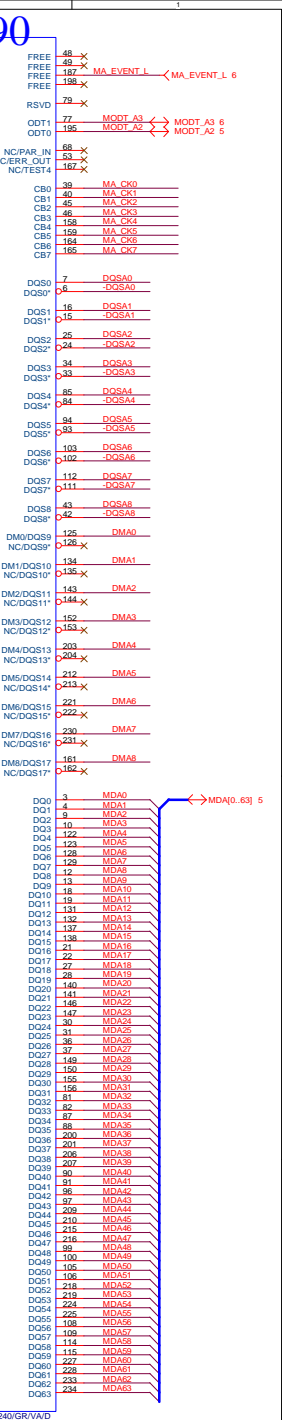
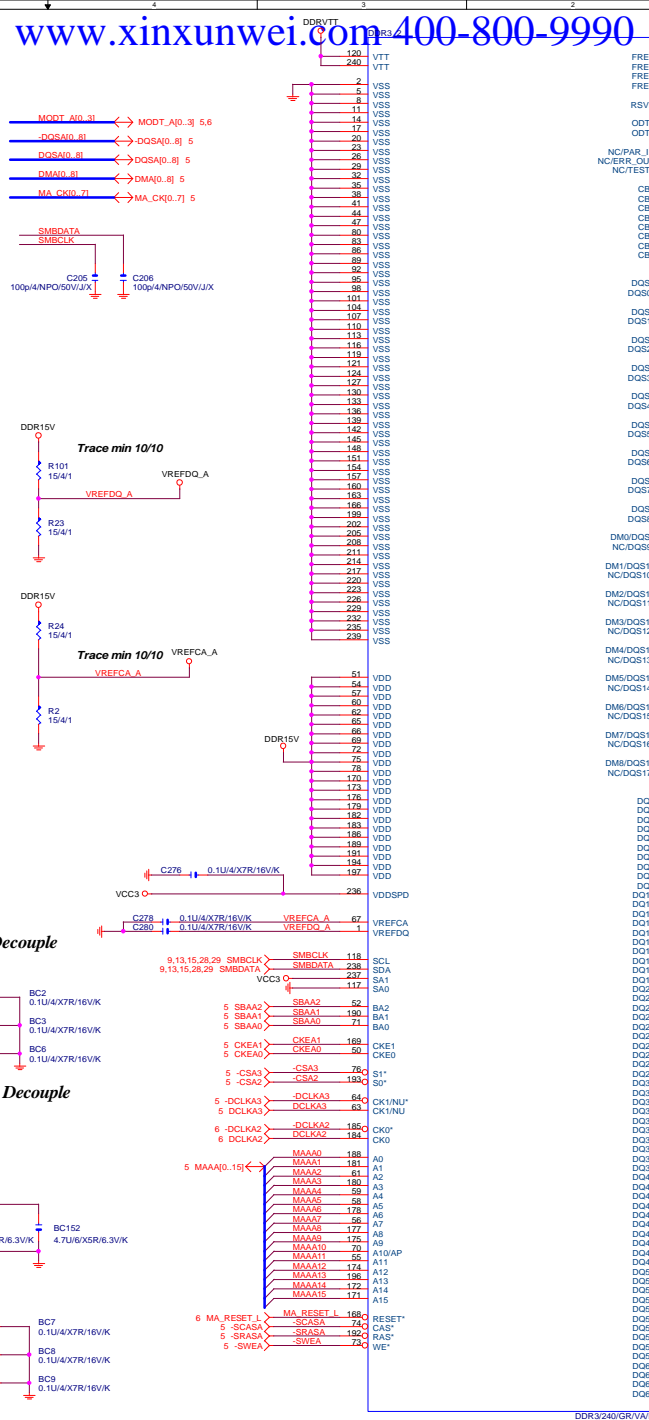
B0 B1

				
Title				
<b>COVER SHEET</b>				
Size	Document Number			Rev
Custom	<b>GA-990FXA-UD3</b>			<b>4.02</b>
Date:	Thursday, July 03, 2014	Sheet	5 of	35

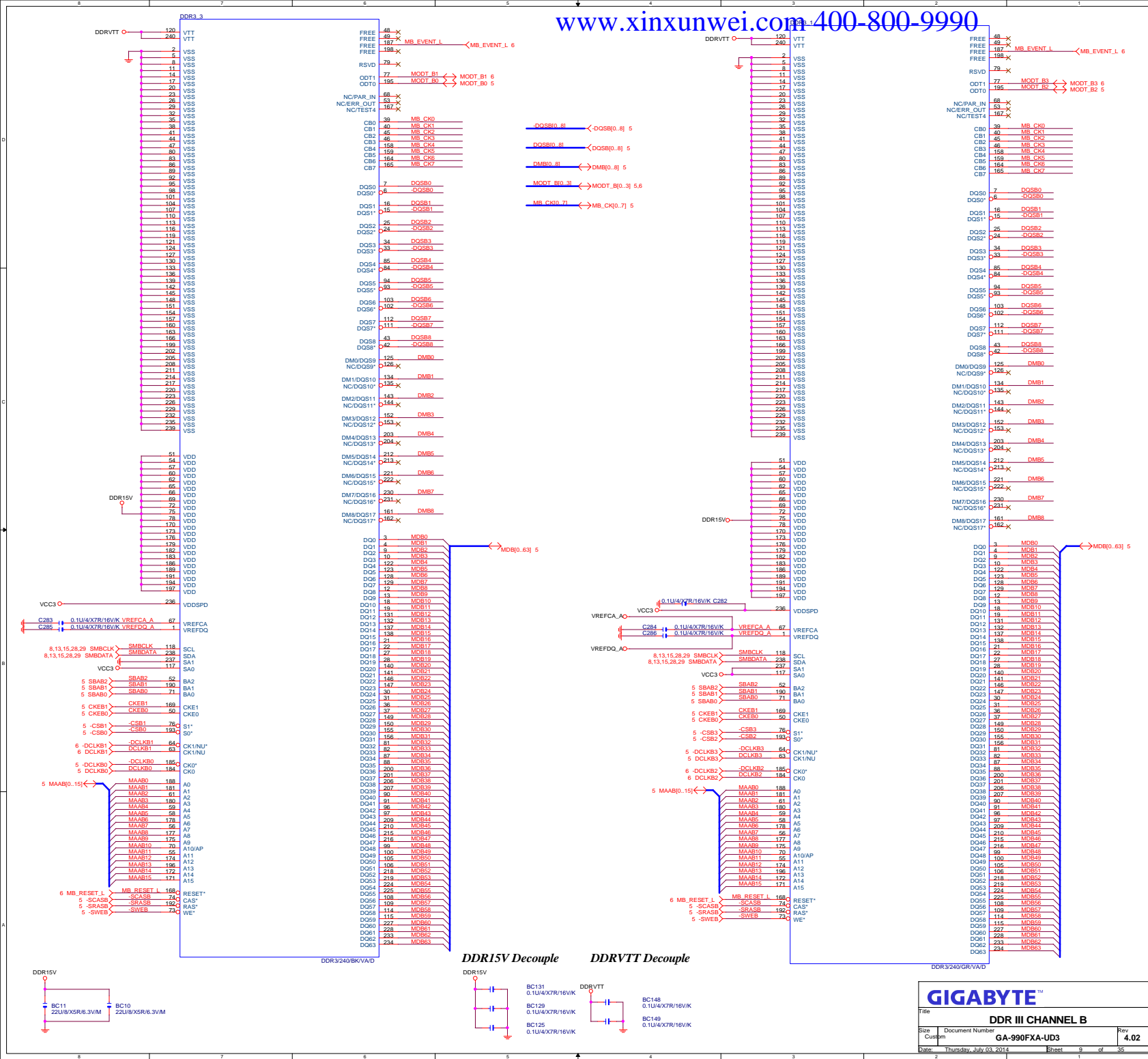












PART 1/5

L0 CADOUT H15	T25	HT RXCAD15P	N23	L0 CADIN H15
L0 CADOUT L15	T24	HT RXCAD15S	N24	L0 CADIN L15
L0 CADOUT L14	U24	HT RXCAD14P	M24	L0 CADIN H14
L0 CADOUT L14	U23	HT RXCAD14S	M25	L0 CADIN L14
L0 CADOUT H13	V25	HT RXCAD14N	L23	L0 CADIN H13
L0 CADOUT L13	V24	HT RXCAD13N	L24	L0 CADIN L13
L0 CADOUT H12	W23	HT RXCAD12P	K24	L0 CADIN H12
L0 CADOUT L12	W24	HT RXCAD12N	K25	L0 CADIN L12
L0 CADOUT H11	AA24	HT RXCAD11P	H24	L0 CADIN H11
L0 CADOUT L11	AA23	HT RXCAD11N	H25	L0 CADIN L11
L0 CADOUT H10	AB24	HT RXCAD10P	G24	L0 CADIN H10
L0 CADOUT L10	AB24	HT RXCAD10N	G24	L0 CADIN L10
L0 CADOUT H9	AC24	HT RXCAD9P	F24	L0 CADIN H9
L0 CADOUT L9	AC23	HT RXCAD9N	F25	L0 CADIN L9
L0 CADOUT H8	AD24	HT RXCAD8P	E24	L0 CADIN H8
L0 CADOUT L8	AD24	HT RXCAD8N	E24	L0 CADIN L8
L0 CADOUT H7	T28	HT RXCAD7P	N26	L0 CADIN H7
L0 CADOUT L7	U27	HT RXCAD7N	M27	L0 CADIN L7
L0 CADOUT H6	U26	HT RXCAD6P	M27	L0 CADIN H6
L0 CADOUT L6	U26	HT RXCAD6N	M28	L0 CADIN L6
L0 CADOUT H5	V28	HT RXCAD5P	L26	L0 CADIN H5
L0 CADOUT L5	V27	HT RXCAD5N	L26	L0 CADIN L5
L0 CADOUT H4	W27	HT RXCAD4N	K27	L0 CADIN H4
L0 CADOUT L4	W26	HT RXCAD4P	K28	L0 CADIN L4
L0 CADOUT H3	AA27	HT RXCAD3N	H27	L0 CADIN H3
L0 CADOUT L3	AA26	HT RXCAD3P	H28	L0 CADIN L3
L0 CADOUT H2	AB28	HT RXCAD3N	G26	L0 CADIN H2
L0 CADOUT L2	AB27	HT RXCAD2P	G27	L0 CADIN L2
L0 CADOUT H1	AC27	HT RXCAD2N	F27	L0 CADIN H1
L0 CADOUT L1	AC26	HT RXCAD1P	F28	L0 CADIN L1
L0 CADOUT H0	AD28	HT RXCAD1N	E26	L0 CADIN H0
L0 CADOUT L0	AD27	HT RXCAD0N	E27	L0 CADIN L0

# HYPERTRANSPORT IF

4	L0_CLKOUT_H1	Y25	HT_RXCLK1P1	HT_TXCLK1P1	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
4	L0_CLKOUT_L1	Y24	HT_RXCLK1N1	HT_TXCLK1N1	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
4	L0_CLKOUT_H0	Y28	HT_RXCLK0P1	HT_TXCLK0P1	J26	L0_CLKIN_H0	L0_CLKIN_H0	4
4	L0_CLKOUT_L0	Y27	HT_RXCLK0N1	HT_TXCLK0N1	J27	L0_CLKIN_L0	L0_CLKIN_L0	4
4	L0_CTLOUT_H1	R24	HT_RXCTL1P1	HT_TXCTL1P1	P24	L0_CTLIN_H1	L0_CTLIN_H1	4
4	L0_CTLOUT_L1	R23	HT_RXCTL1N1	HT_TXCTL1N1	P25	L0_CTLIN_L1	L0_CTLIN_L1	4
4	L0_CTLOUT_H0	R27	HT_RXCTL0P1	HT_TXCTL0P1	P27	L0_CTLIN_H0	L0_CTLIN_H0	4
4	L0_CTLOUT_L0	R26	HT_RXCTL0N1	HT_TXCTL0N1	P28	L0_CTLIN_L0	L0_CTLIN_L0	4

SNR0 1.21K/4/1 HT\_RXCALP D25 HT\_RXCALP D24 HT\_TXCALP D28 HT\_TXCALP NR1 1.21K/4/1

RD990/BGA692

**L0\_CADIN\_H[0..15]** → **L0\_CADIN\_H[0..15]** 4

L0\_CADIN\_L[0..15] → L0\_CADIN\_L[0..15] 4

```
4 L0_CADOUT_H[0..15] ← L0_CADOUT_H[0..15]
```

```
4 L0_CADOUT_L[0..15] <= L0_CADOUT_L[0..15]
```

EXP\_A\_RXP[0..15] >> EXP\_A\_RXP[0..15] 18

EXP\_A\_RXN[0..15] >> EXP\_A\_RXN[0..15] 18

```

EXP_A_TXN[0..15]  >> EXP_A_TXP[0..15]  18
EXP_A_TXN[0..15]  >> EXP_A_TXN[0..15]  18

```

EXP\_B\_TXP[0..15] >> EXP\_B\_TXP[0..15] 19

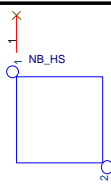
EXP\_B\_TXN[0..15] >> EXP\_B\_TXN[0..15] 19

EXP\_B\_RXP[0..15] >> EXP\_B\_RXP[0..15] 19

EXP\_B\_RXN[0..15] 19

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**N.B HEATSINK**



NB\_HS/[12SP2-070018-01R\_12SP2-070018-02R]/X

## PART 2/5

EXP A RXP15	N6	GPP1 RX15P	GPP1 TX15S	N3	EXP A TXP15
EXP A RXN15	N5	GPP1 RX15P	GPP1 TX15N	N2	EXP A TXN15
EXP A RXP14	M5	GPP1 RX14P	GPP1 TX14P	M2	EXP A TXP14
EXP A RXN14	M4	GPP1 RX14P	GPP1 TX14N	M1	EXP A TXN14
EXP A RXP13	L6	GPP1 RX14N	GPP1 TX12P	L3	EXP A TXP13
EXP A RXN13	L5	GPP1 RX13P	GPP1 TX12N	L2	EXP A TXN13
EXP A RXP12	K5	GPP1 RX13P	GPP1 TX11P	K2	EXP A TXP12
EXP A RXN12	K4	GPP1 RX13N	GPP1 TX11N	J3	EXP A TXN12
EXP A RXP11	J6	GPP1 RX12P	GPP1 TX12N	J2	EXP A TXP11
EXP A RXN11	J5	GPP1 RX11P	GPP1 TX11P	J1	EXP A TXN11
EXP A RXP10	H5	GPP1 RX11P	GPP1 TX11N	H2	EXP A TXP10
EXP A RXN10	H4	GPP1 RX10P	GPP1 TX10P	H1	EXP A TXN10
EXP A RXP9	G6	GPP1 RX10N	GPP1 TX10N	G2	EXP A TXP9
EXP A RXN9	G5	GPP1 RXP9	GPP1 TX9P	G1	EXP A TXN9
EXP A RXP8	F6	GPP1 RX9N	GPP1 TX8N	F2	EXP A TXP8
EXP A RXN8	F5	GPP1 RXP8P	GPP1 TX8P	F1	EXP A TXN8
EXP A RXP7	D2	GPP1 RX8N	GPP1 TX8N	E3	EXP A TXP7
EXP A RXN7	D1	GPP1 RXP7P	GPP1 TX7P	E2	EXP A TXN7
EXP A RXP6	B5	GPP1 RX7N	GPP1 TX7N	A4	EXP A TXP6
EXP A RXN6	B6	GPP1 RXP6P	GPP1 TX6P	B4	EXP A TXN6
EXP A RXP5	D6	GPP1 RX6N	GPP1 TX6N	A6	EXP A TXP5
EXP A RXN5	E6	GPP1 RXP5P	GPP1 TX5P	B7	EXP A TXN5
EXP A RXP4	E7	GPP1 RX5N	GPP1 TX5N	B6	EXP A TXP4
EXP A RXN4	F7	GPP1 RX4P	GPP1 TX4P	C7	EXP A TXN4
EXP A RXP3	D8	GPP1 RX4N	GPP1 TX4N	A8	EXP A TXP3
EXP A RXN3	E8	GPP1 RXP3P	GPP1 TX3P	B8	EXP A TXN3
EXP A RXP2	F9	GPP1 RX3N	GPP1 TX3N	C9	EXP A TXP2
EXP A RXN2	E9	GPP1 RX2P	GPP1 TX2P	A9	EXP A TXN2
EXP A RXP1	D10	GPP1 RX2N	GPP1 TX2N	A10	EXP A TXP1
EXP A RXN1	E10	GPP1 RX1P	GPP1 TX1P	B10	EXP A TXN1
EXP A RXP0	F11	GPP1 RX1N	GPP1 TX1N	B11	EXP A TXP0
EXP A RXN0	E11	GPP1 RX0P	GPP1 TX0P	C11	EXP A TXN0
		GPP1 RX0N	GPP1 TX0N		

PCIE  
GPP1

EXP B RXP15	AC3	GP22 RX15P5	GP22_TX15S	AF9	EXP B TXP15
EXP B RXN15	AD3	GP22 RX15D	GP22_TX15D	AG8	EXP B TXN15
EXP B RX14	A7	GP22 RX14P	GP22_TX14P	AG7	EXP B TX14
EXP B RXN14	A8	GP22 RX14N	GP22_TX14N	AF7	EXP B TXN14
EXP B RXP13	A6B	GP22 RX13P	GP22_TX13P	AG7	EXP B TXP13
EXP B RXN13	AD7	GP22 RX13N	GP22_TX13N	AG6	EXP B TXN13
EXP B RX12	AD3	GP22 RX12P	GP22_TX12P	AG8	EXP B TX12
EXP B RXN12	A6B	GP22 RX12N	GP22_TX12N	AG6	EXP B TXN12
EXP B RXP11	AF5	GP22 RX11P	GP22_TX11P	AG4	EXP B TXP11
EXP B RXN11	AE5	GP22 RX11N	GP22_TX11N	AH4	EXP B TXN11
EXP B RXP10	AE2	GP22 RX10P	GP22_TX10P	AE3	EXP B TXP10
EXP B RXN10	AE1	GP22 RX10N	GP22_TX10N	AE2	EXP B TXN10
EXP B RXP9	AD1	GP22 RX9P	GP22_TX9P	AC3	EXP B TXP9
EXP B RXN9	AD1	GP22 RX9N	GP22_TX9N	AC2	EXP B TXN9
EXP B RXP8	AB5	GP22 RX8P	GP22_TX8P	AB2	EXP B TXP8
EXP B RXN8	AB4	GP22 RX8N	GP22_TX8N	AB1	EXP B TXN8
EXP B RXP7	AA6	GP22 RX7P	GP22_TX7P	AA2	EXP B TXP7
EXP B RXN7	AA5	GP22 RX7N	GP22_TX7N	Y3	EXP B TXN7
EXP B RXP6	Y5	GP22 RX6P	GP22_TX6P	Y2	EXP B TXP6
EXP B RXN6	Y4	GP22 RX6N	GP22_TX6N	Y1	EXP B TXN6
EXP B RXP5	W6	GP22 RX5P	GP22_TX5P	W3	EXP B TXP5
EXP B RXN5	W5	GP22 RX5N	GP22_TX5N	W2	EXP B TXN5
EXP B RXP4	V5	GP22 RX4P	GP22_TX4P	V2	EXP B TXP4
EXP B RXN4	V4	GP22 RX4N	GP22_TX4N	V1	EXP B TXN4
EXP B RXP3	U5	GP22 RX3P	GP22_TX3P	U3	EXP B TXP3
EXP B RXN3	U3	GP22 RX3N	GP22_TX3N	U2	EXP B TXN3
EXP B RXP2	T5	GP22 RX2P	GP22_TX2P	T2	EXP B TXP2
EXP B RXN2	T4	GP22 RX2N	GP22_TX2N	T1	EXP B TXN2
EXP B RXP1	Q6	GP22 RX1P	GP22_TX1P	R3	EXP B TXP1
EXP B RXN1	R5	GP22 RX1N	GP22_TX1N	R2	EXP B TXN1
EXP B RXP0	P5	GP22 RX0P	GP22_TX0P	P2	EXP B TXP0
EXP B RXN0	P4	GP22 RX0N	GP22_TX0N	P1	EXP B TXN0

pp6IE  
GPP2

AD11	GPP3_RX9P	GPP3_TX9P	AH10	GPP_TX9P_C	C6
AD12	GPP3_RX9N	GPP3_TX9N	AH10	GPP_TX9N_C	C5
AE12	GPP3_RX8P	GPP3_TX8P	AH11	GPP_TX8P_C	C7
AD13	GPP3_RX8N	GPP3_TX8N	AH12	GPP_TX8P_C	C8
AC13	GPP3_RX7P	GPP3_TX7P	AH12	GPP_TX7P_C	C11
AE14	GPP3_RX7N	GPP3_TX7N	AH12	GPP_TX7N_C	C12
AD14	GPP3_RX6P	GPP3_TX6P	AH13	GPP_TX6P_C	C14
AD15	GPP3_RX5P	GPP3_TX5N	AH13	GPP_TX6N_C	C15
AC15	GPP3_RX5N	GPP3_TX6N	AH14	GPP_TX5P_C	C14
AE16	GPP3_RX4P	GPP3_TX4N	AH14	GPP_TX5N_C	NC4
AD16	GPP3_RX4N	GPP3_TX4P	AH15	GPP_TX4P_C	NC6
AD17	GPP3_RX3P	GPP3_TX3N	AH15	GPP_TX4N_C	NC5
AE18	GPP3_RX3N	GPP3_TX2P	AH16	GPP_TX3P_C	NC7
AD18	GPP3_RX2N	GPP3_TX2N	AH16	GPP_TX3N_C	NC8
AD19	GPP3_RX1P	GPP3_TX1P	AE17	GPP_TX2N_C	NC1
AC19	GPP3_RX1N	GPP3_TX1N	AH17	GPP_TX1P_C	NC2
AH20	GPP3_RX0P	GPP3_TX0P	AH18	GPP_TX1N_C	NC3
AG20	GPP3_RX0N	GPP3_TX0N	AE19	GPP_TX0P_C	NC4
			AH19	GPP_TX0N_C	NC1

## ALINK

AC21	SB, RX3P	AG22	A, TX3P	C	NC1
AD21	SB, RX3N	AH22	A, TX3N	C	NC1
AD22	SB, RX2P	A21	A, TX2P	C	NC1
AE22	SB, RX2N	AF21	A, TX2N	C	NC1
AF25	SB, RX2N	AF23	A, TX1P	C	NC1
AG25	SB, RX1P	AG23	A, TX1N	C	NC1
AG26	SB, RX1N	AH24	A, TX0P	C	NC1
AH26	SB, RX0P	AG24	A, TX0N	C	NC1
AE26	SB, RX0N	SB, TX0P			
		SB, TX0N			

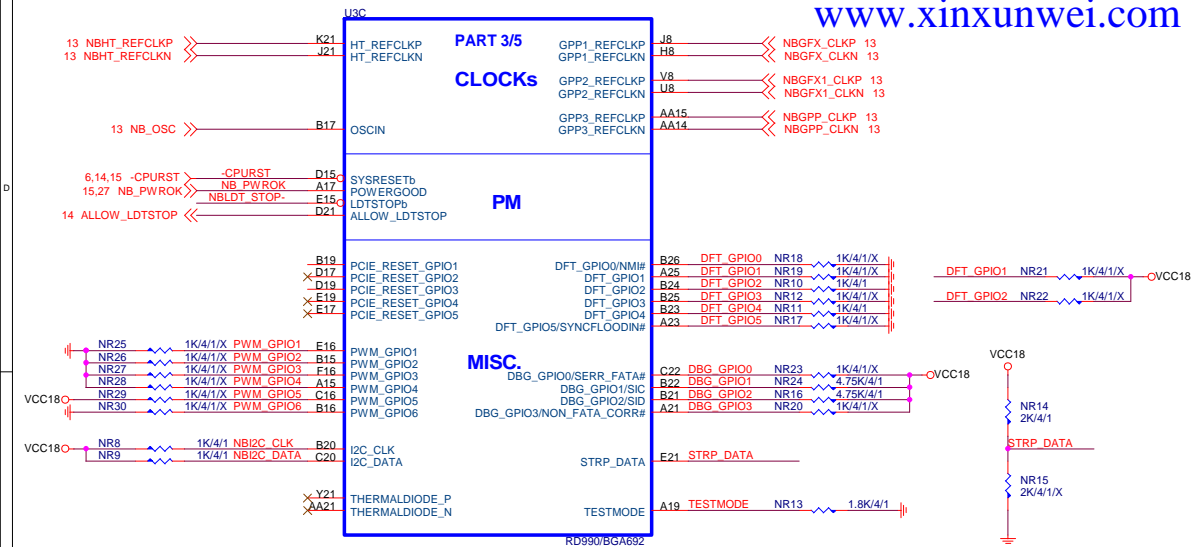
PLACE THESE CAP CLOSE TO NB.

**GIGABYTE™**

Title	RD990 HT & GFX I/F
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Size Custom	Document Number <b>GA-990FXA-UD3</b>	Rev <b>4.02</b>
Date:	Thursday, July 03, 2014	Sheet 10 of 35

RD990/BGA692

**DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO.  
 1 : Disable ( Can still be enabled using nbcfg register access)  
 0 : Enable

**DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]**

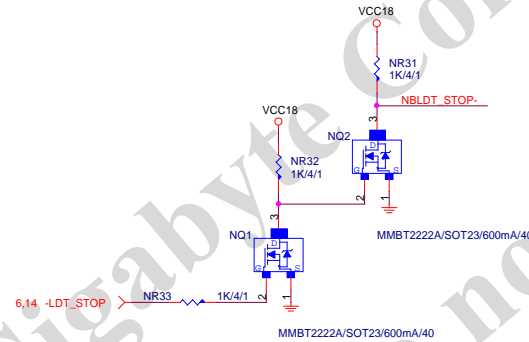
These pin straps are used to configure PCI-E GPP mode.  
**GPIO4:3:2**  
**000** : 4:2:4 B  
**001** : 4:1:1:4 C  
**010** : 1:1:1:1:1:4 L (Hardware Default)  
**011** : 2:1:1:1:1:4 E  
**100** : 2:2:1:1:4 K  
**101** : 2:2:2:4 C2  
**110** : Hardware default (mode L) or EEPROM  
**111** : Hardware default (mode L) or EEPROM  
**101** : 01100  
**111** : 01011

**DFT\_GPIO1: LOAD\_EEPROM\_STRAPS**

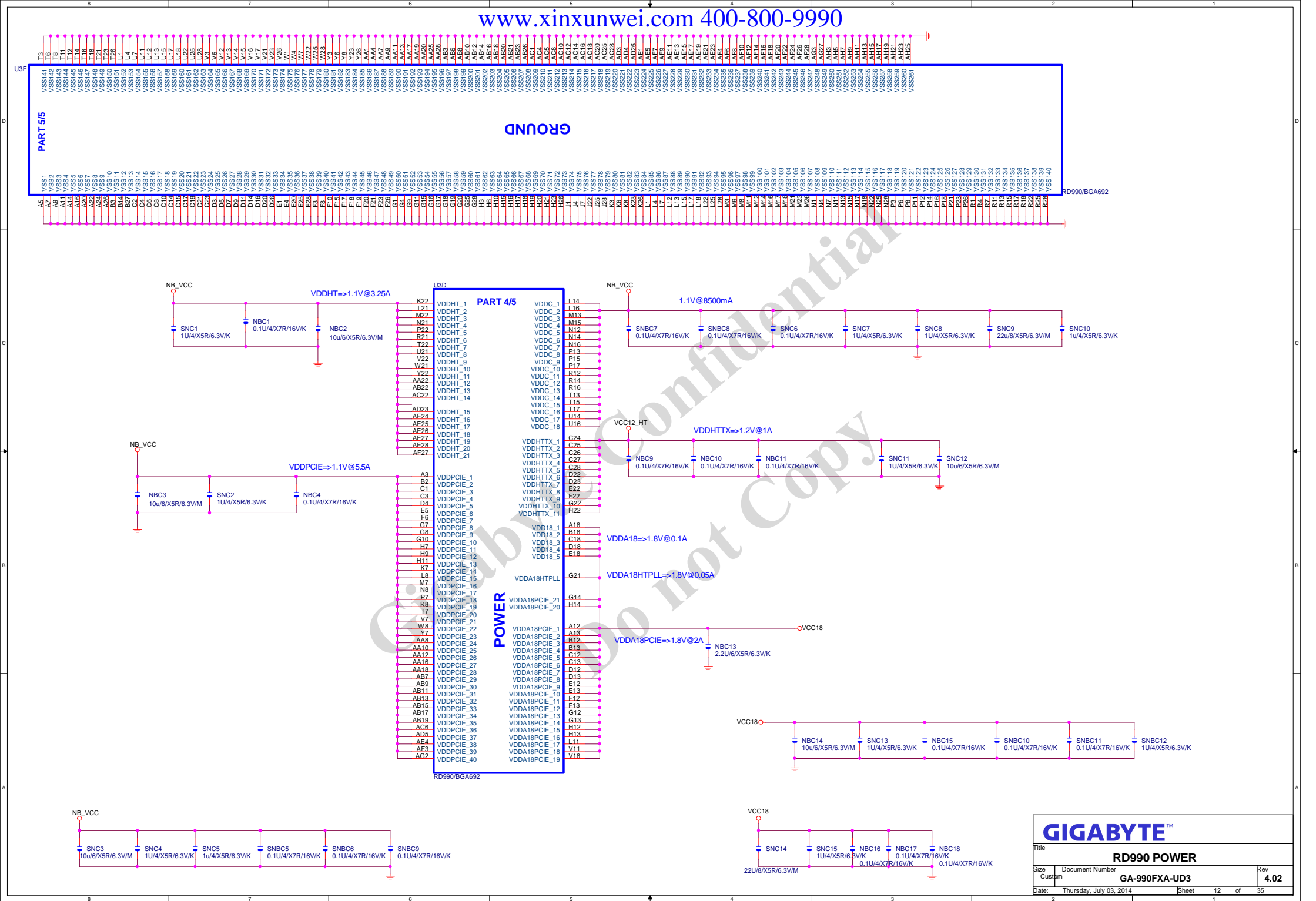
Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

**DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb**

Enables the Test Debug Bus using PCIE bus  
 1 : Disable ( Can still be enabled using nbcfg register access )  
 0 : Enable

**GIGABYTE™**

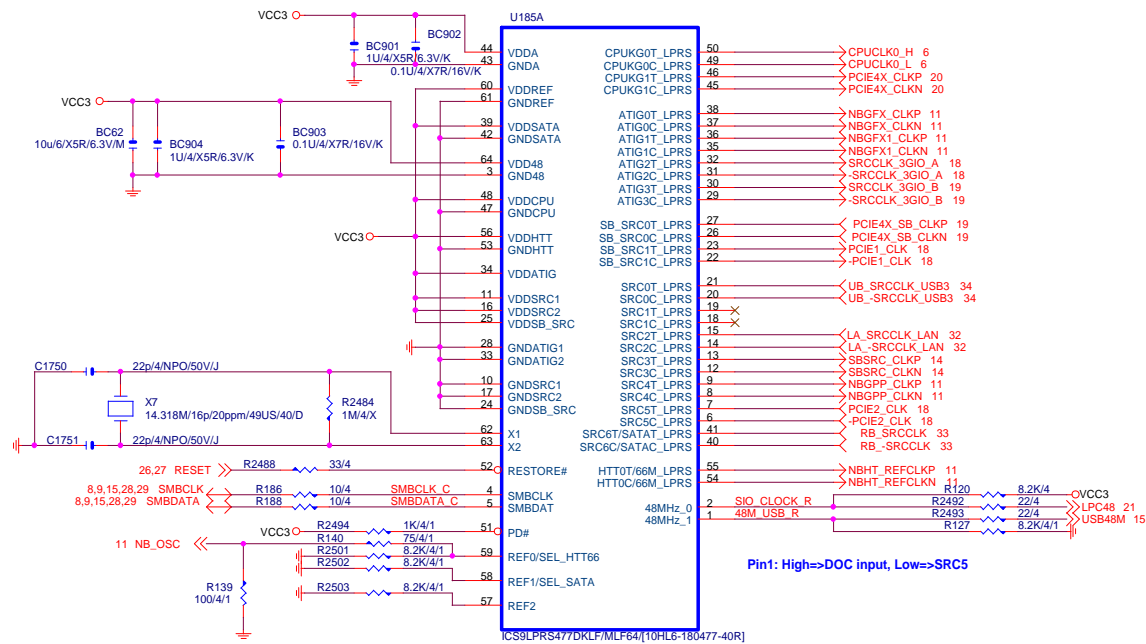
Title		<b>RD990 CLOCK &amp; SYSB I/F</b>	
Size	Document Number	Rev	
Custom	<b>GA-990FXA-UD3</b>	<b>4.02</b>	
Date:	Thursday, July 03, 2014	Sheet	11 of 35



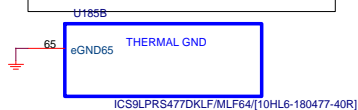
## NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

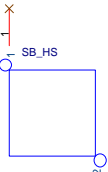
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE™

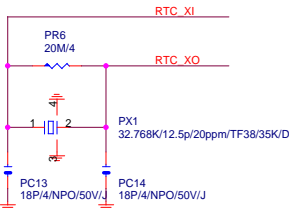
Title	ICS9LPRS477		
Size	Document Number	Rev	
Custm	GA-990FXA-UD3	4.02	
Date:	Thursday, July 03, 2014	Sheet	13 of 35

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

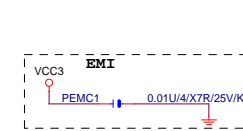
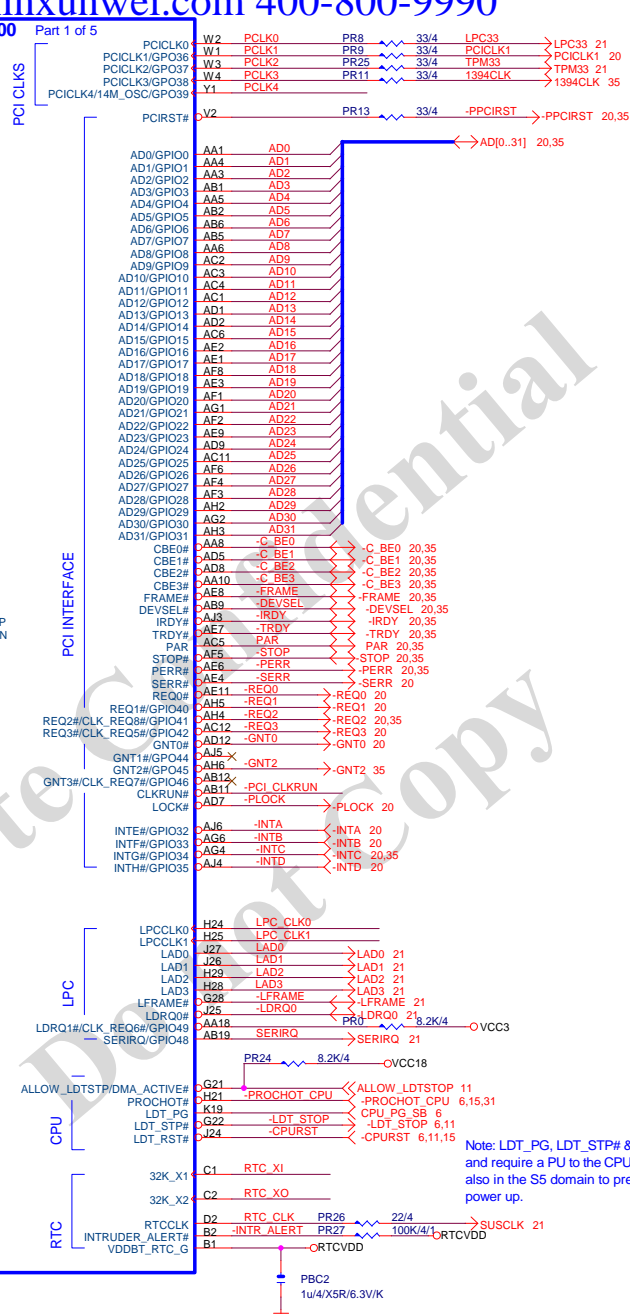
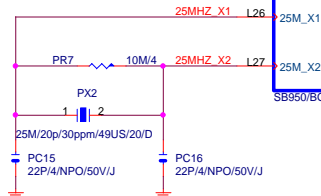
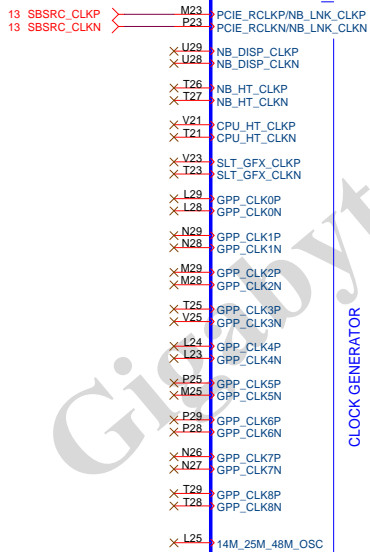
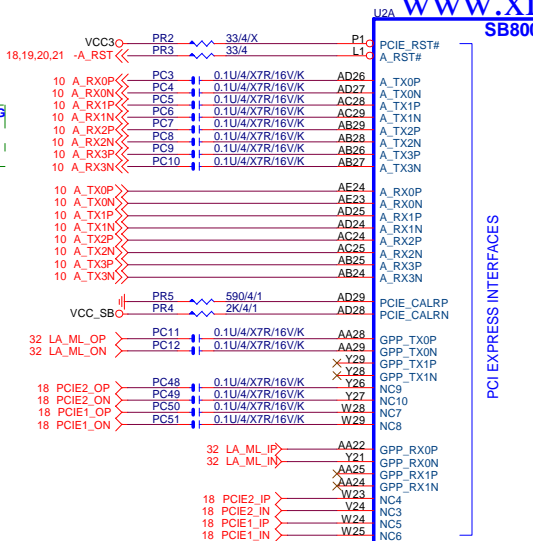
S.B HEATSINK



SB\_HS/[12SP2-SA0704-01R\_12SP2-SA0704-02R\_12SP2-SA0704-03R]



PX1   
SHW/D0.64\*5.08\*6.74



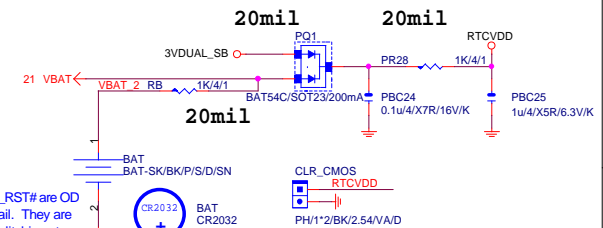
Low: Force PCIE GEN1, Up: Allow PCIE GEN2

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting  
EC AOD-ACC



	LPC CLK0 Rev.AT2	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	AOD Extreme IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

**NOT ADD ICT FOR RTCVDD PIN**

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Title	ATI SB950 PCIE/PCI/CPU/LPC
-------	----------------------------

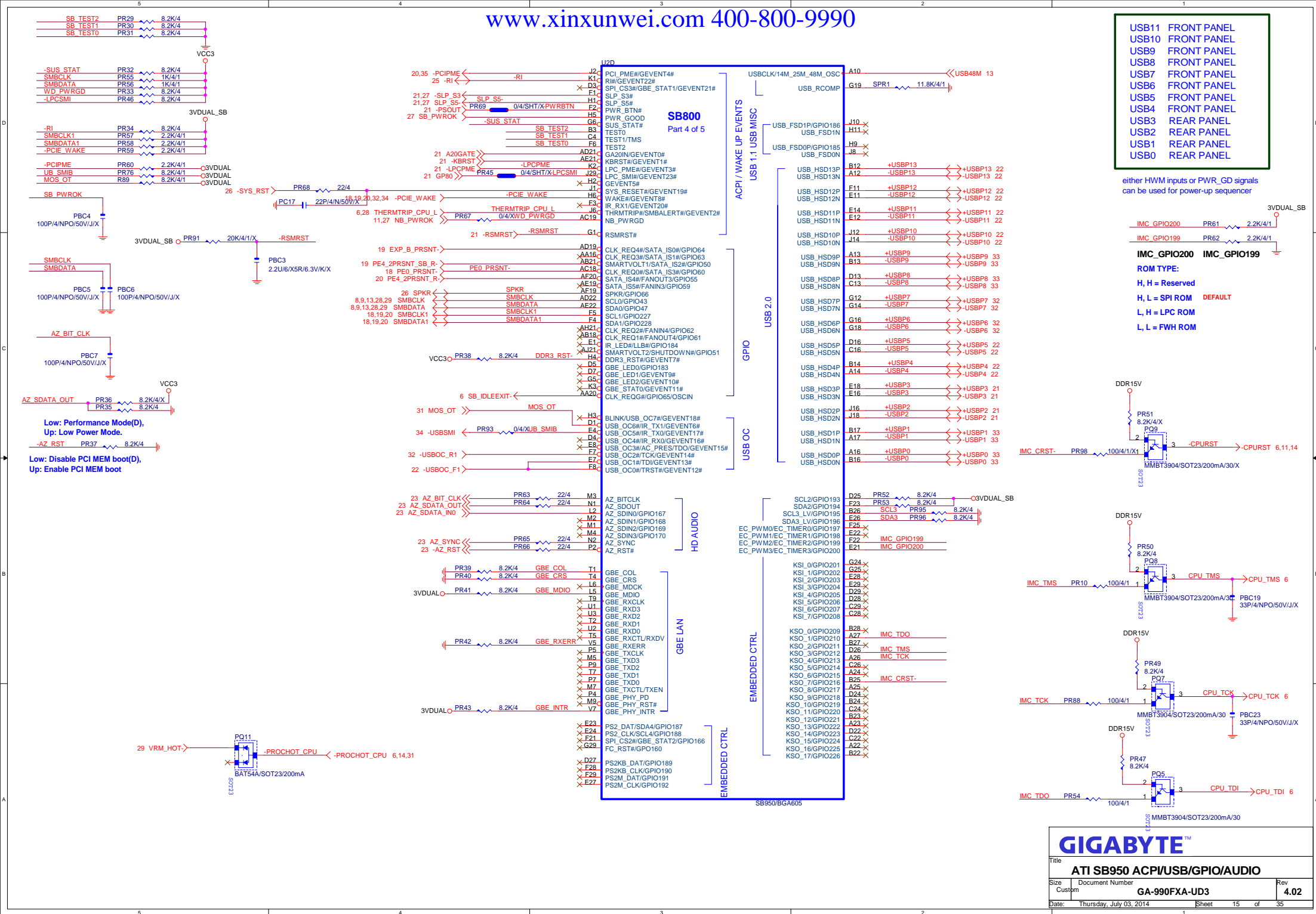
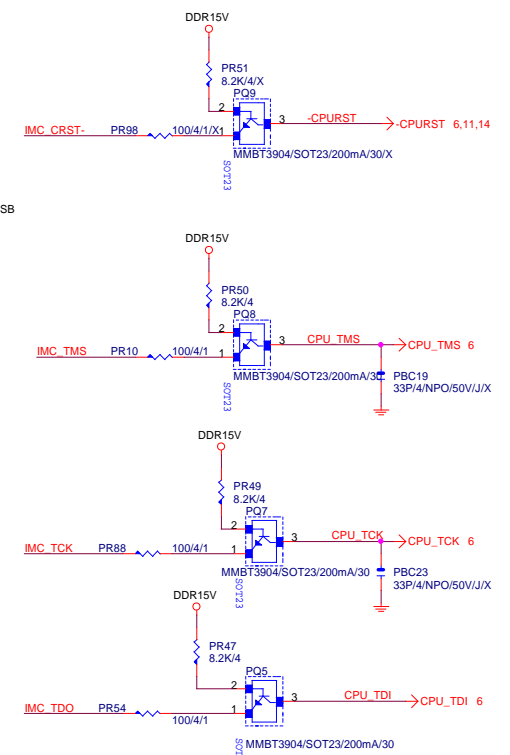
Size	Document Number	Rev
Custom	<b>GA-990FXA-UD3</b>	<b>4.02</b>
Date:	Thursday, July 03, 2014	Sheet 14 of 35

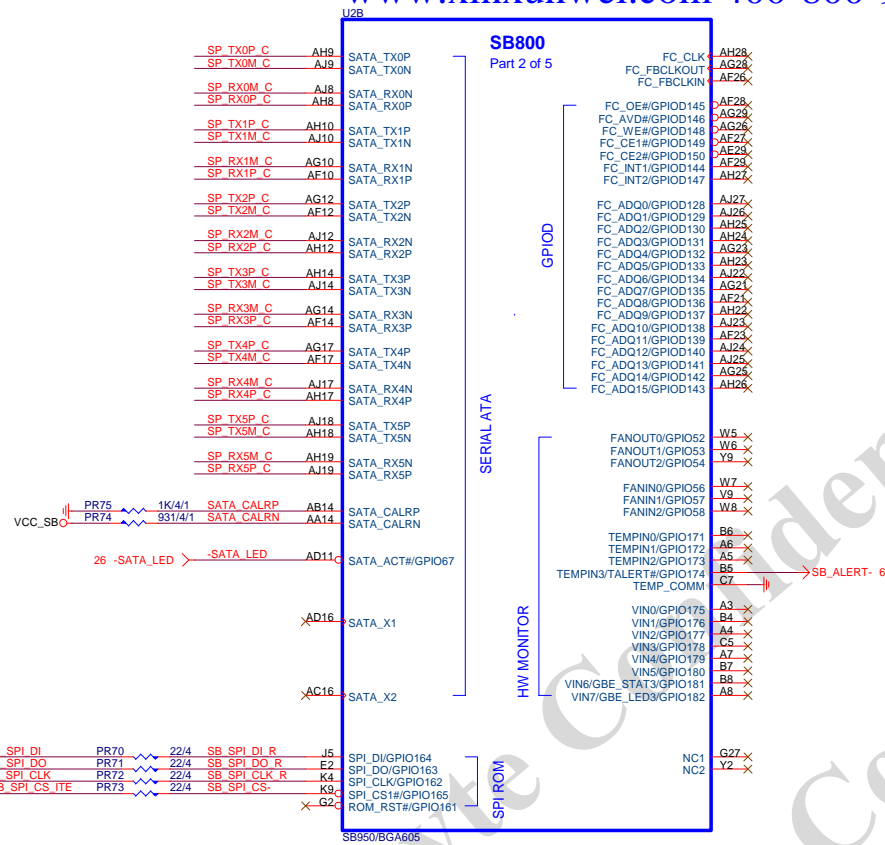


USB11 FRONT PANEL  
 USB10 FRONT PANEL  
 USB9 FRONT PANEL  
 USB8 FRONT PANEL  
 USB7 FRONT PANEL  
 USB6 FRONT PANEL  
 USB5 FRONT PANEL  
 USB4 FRONT PANEL  
 USB3 REAR PANEL  
 USB2 REAR PANEL  
 USB1 REAR PANEL  
 USB0 REAR PANEL

either HWM inputs or PWR\_GD signals  
 can be used for power-up sequencer

IMC\_GPIO200 PR61 2.2K/4/1  
 IMC\_GPIO199 PR62 2.2K/4/1  
**IMC\_GPIO200 IMC\_GPIO199**  
**ROM TYPE:**  
 H, H = Reserved  
 L, L = SPI ROM **DEFAULT**  
 L, H = LPC ROM  
 L, L = FWH ROM





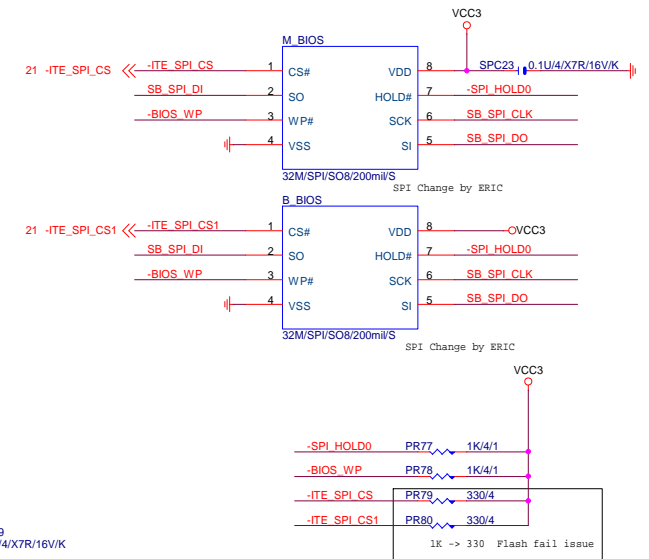
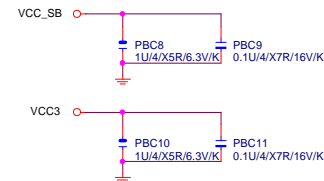
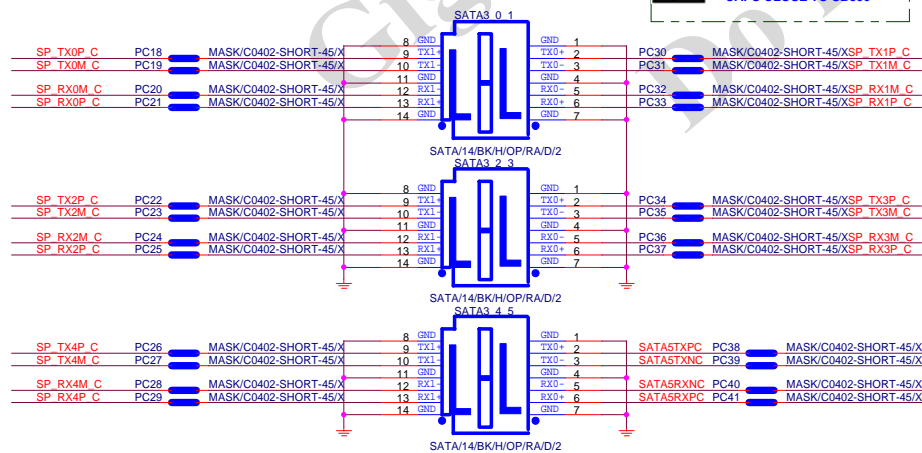
PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF U600

#### NOTE:

R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK

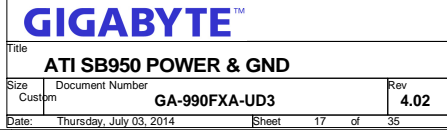


PLACE SATA AC COUPLING  
CAPS CLOSE TO SB850

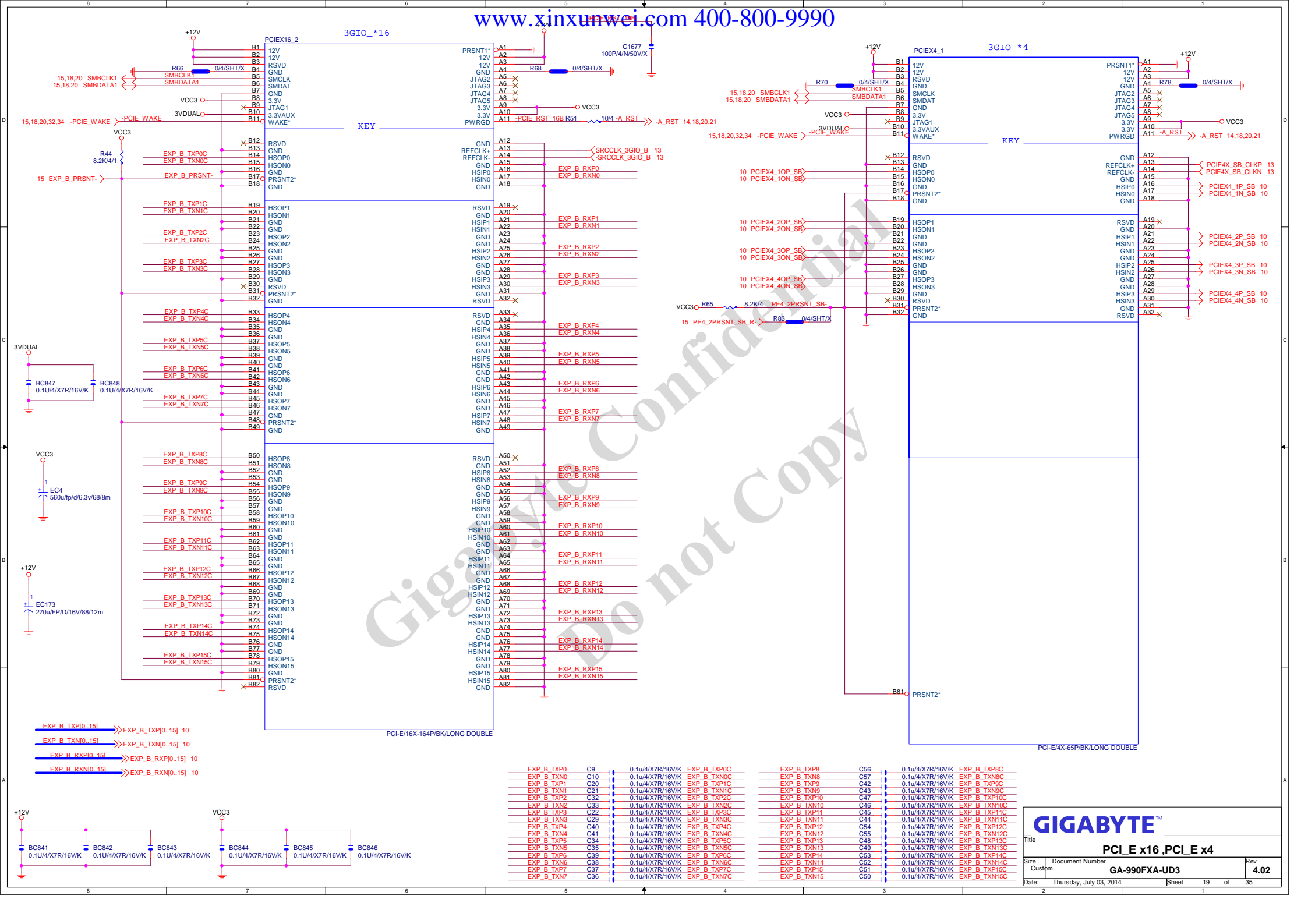


**GIGABYTE**

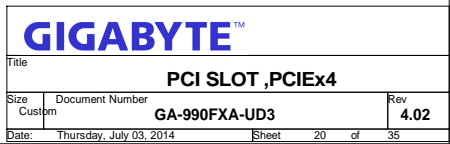
Title		
ATI SB950 SATA/IDE/HWM/SPI		
Size		Rev
Custom	Document Number	4.02
Date: Thursday, July 03, 2014		Sheet 16 of 35



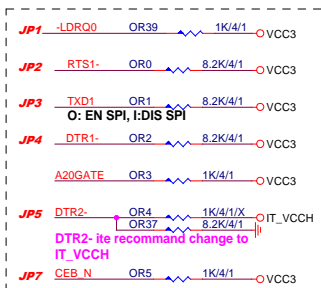
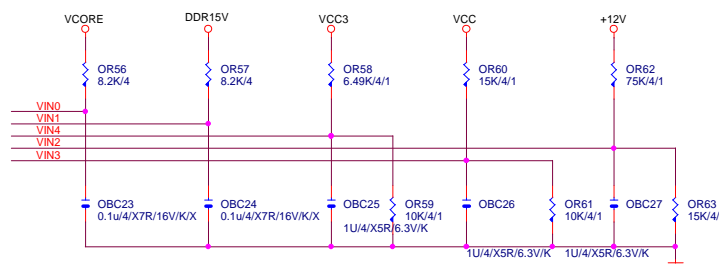
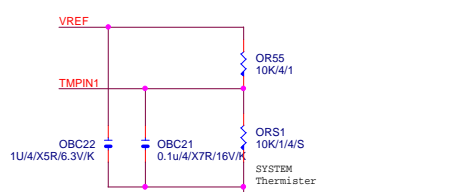
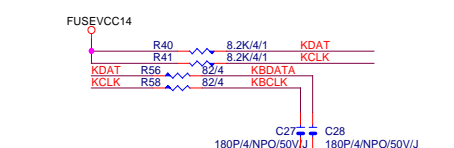
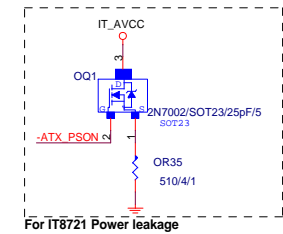




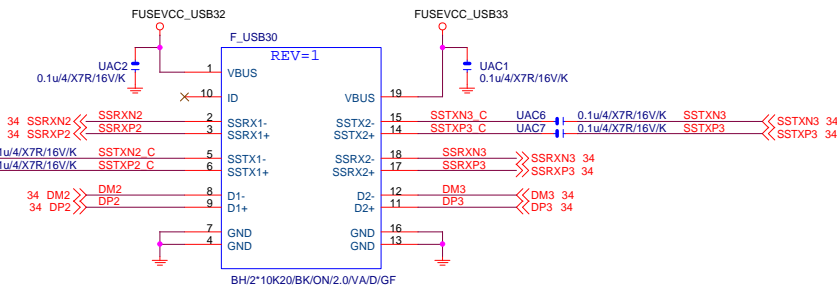
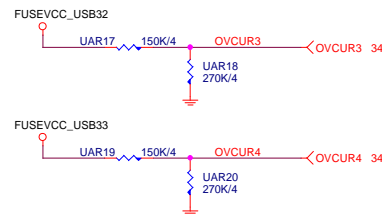
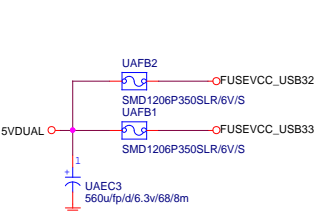
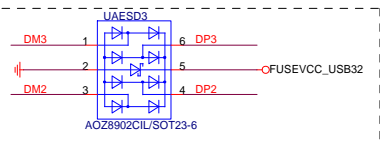
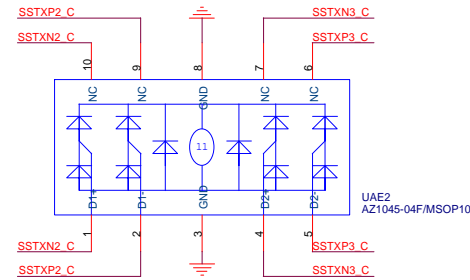
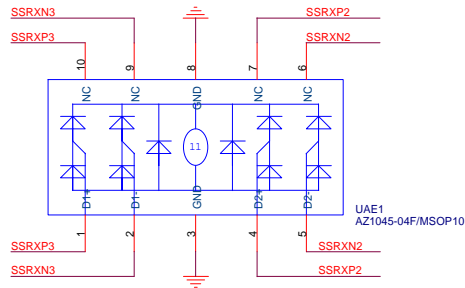
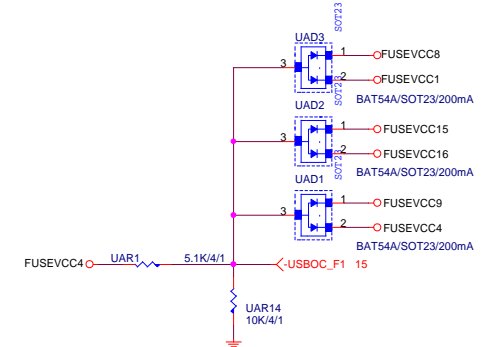
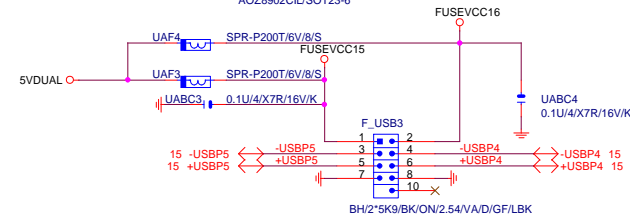
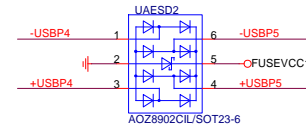
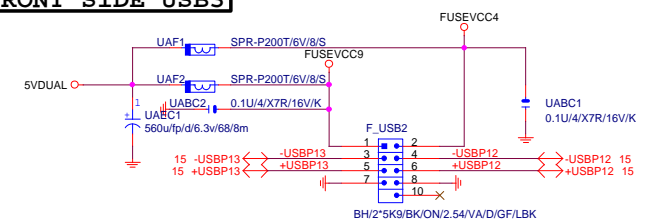
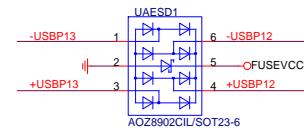
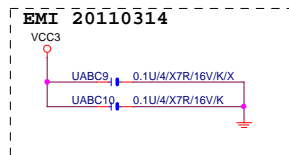




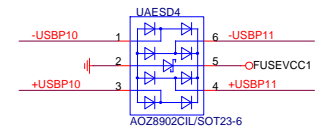
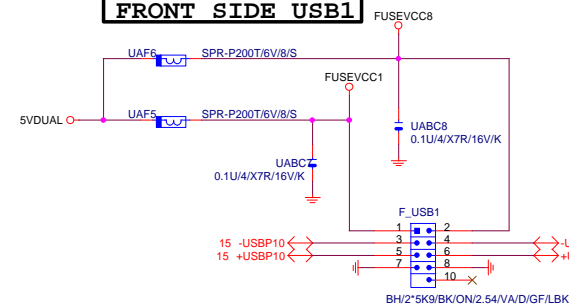




## FRONT SIDE USB3



## FRONT SIDE USB1



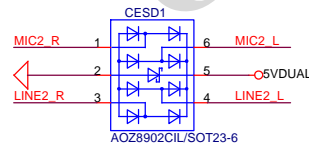
GIGABYTE™

Title		COM/LPT/F_USB	
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	4.02	
Date:	Thursday, July 03, 2014	Sheet	22 of 35

	ALC889	ALC889B	ALC898/ALC892
CR65	O	O	X
CBC35	X	X	10uF/X5R
CBC39	X	10uF/X5R	X
CR31	O	X	O
CR66	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC5/CBC6/CBC9/CBC11	10uF/X5R	10uF/X5R	10uF/X5R
CR51/CD1/CBC7	X	X	O
CD2/CD3/CQ3/CQ5	O	O	X
CR5/CR8/CR1/CR14/ CR17/CR22/CR45/CR33/ CR47/CR40/CR26/CR37/ CR13/CR11/CR57/CR53	62 ohm	62 ohm	62 ohm

## ALC889/VT2021 Colay

	ALC889	VT2021
CR49	O	O
CBC36	X	X
CR28/CBC11	47ohm+1nF	47ohm+1nF
CR52	O	O
CBC1/CBC2	22uF/X5R	10uF/X5R
CR36	20K/4/1	5.1K/4/1
CBC38/CBC39	X	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR43/CR22/ CR27/CR26	22K/4	10K/4/1
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47 CR2/CR11/CR14/CR24	62 ohm	75 ohm
CFB1/CD1/CBC4	X	X
CD2/CD3/CQ3/CQ4	O	O



co-layout

24 SPDIF02\_HDMI

24 SPDIF03\_HDMI

15 AZ\_SDATA\_OUT

15 AZ\_BIT\_CLK

15 AZ\_SYNC

15 -AZ\_RST

CR60/CBC32 close to PCH

CBC31

22p4/NPO/50V/J/X

Digital Area

Analog Area

JD resistors close to pin13 of CODEC

24 FRONT\_JD

24 LINE1\_JD

24 MIC1\_JD

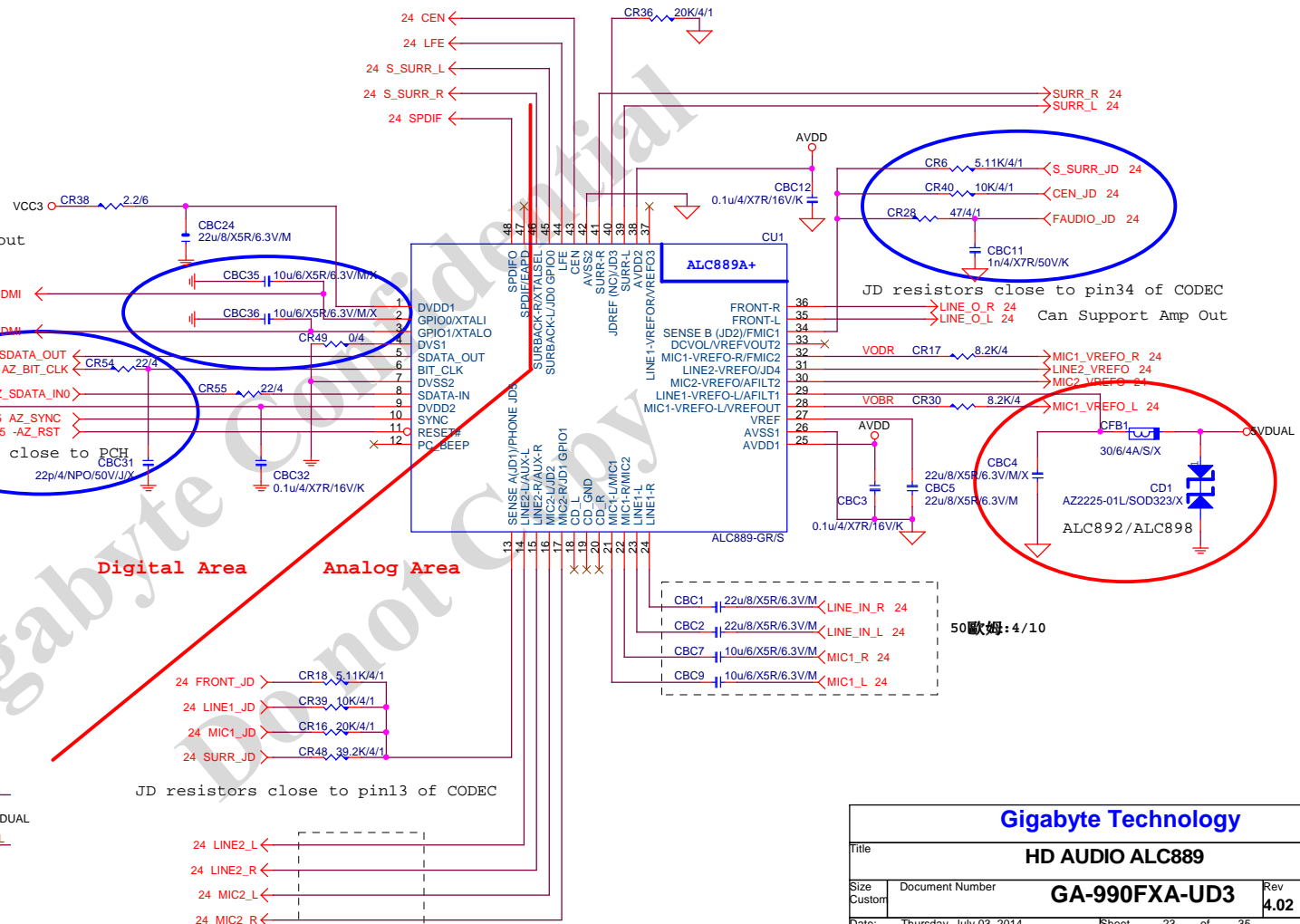
24 SURR\_JD

24 LINE2\_L

24 LINE2\_R

24 MIC2\_L

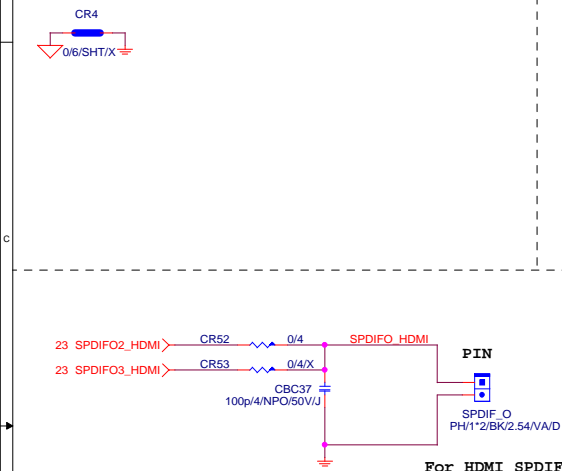
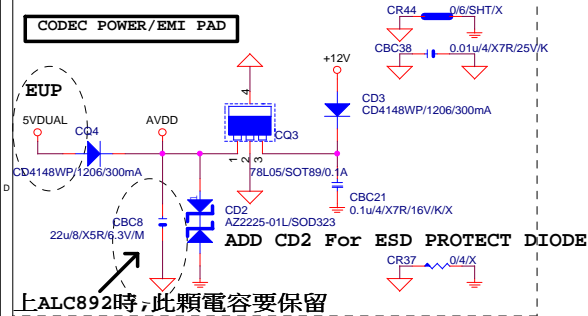
24 MIC2\_R



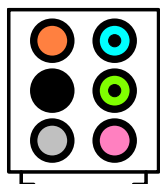
Gigabyte Technology

HD AUDIO ALC889

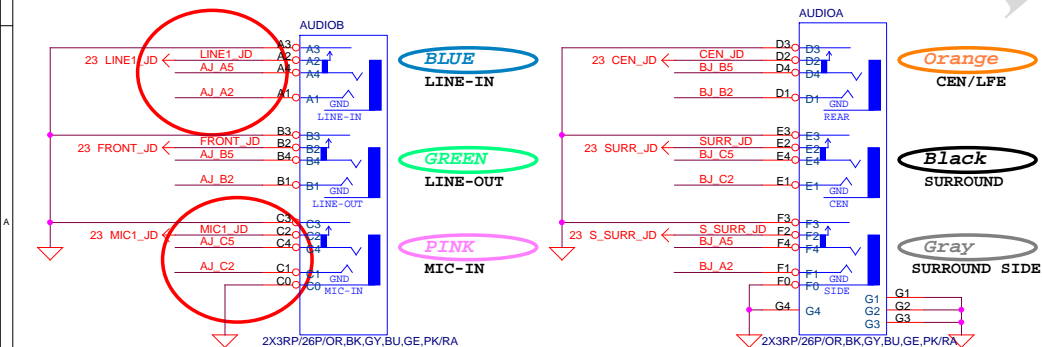
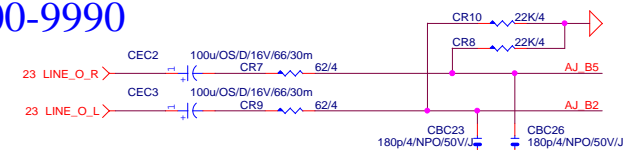
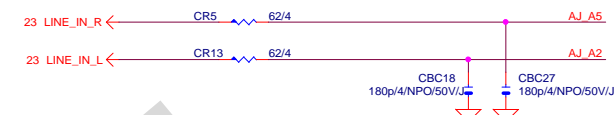
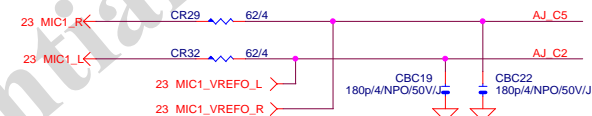
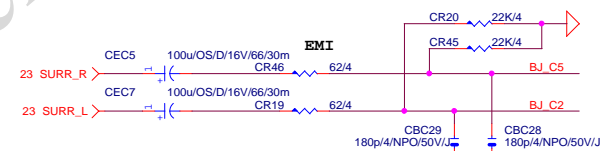
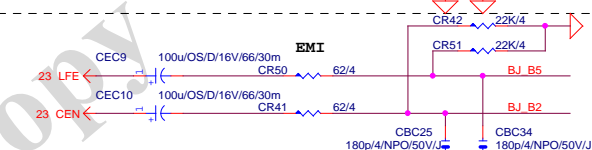
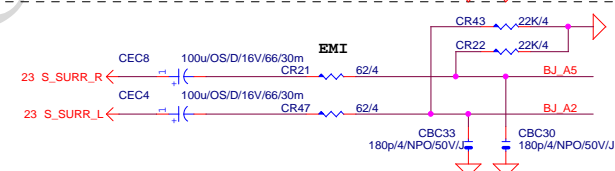
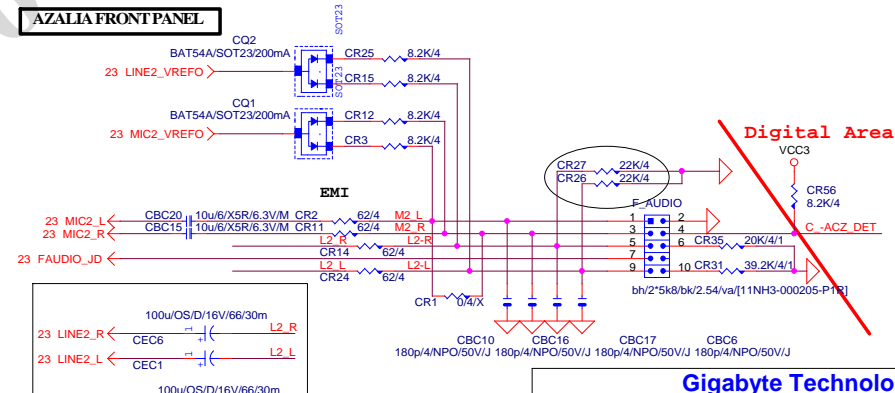
Title	Document Number	Rev
	GA-990FXA-UD3	4.02
Size	Custom	
Date:	Thursday, July 03, 2014	Sheet 23 of 35



**AZALIA JACK**  
BTX AZALIA CONNECTOR

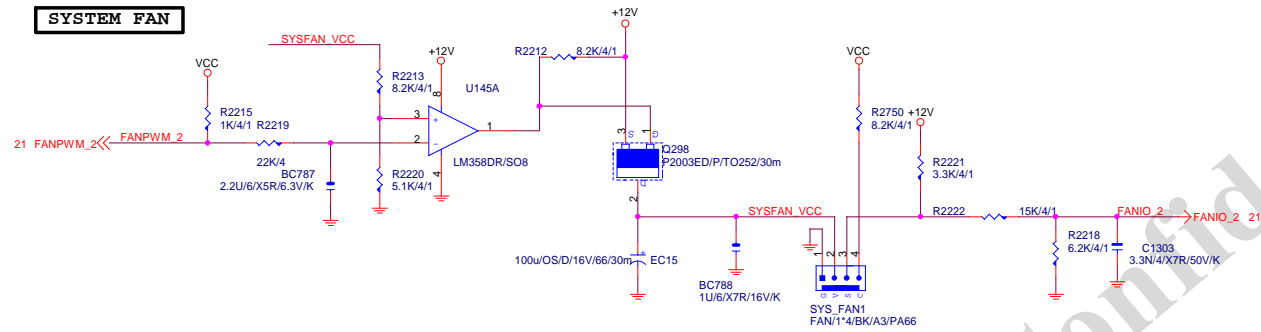
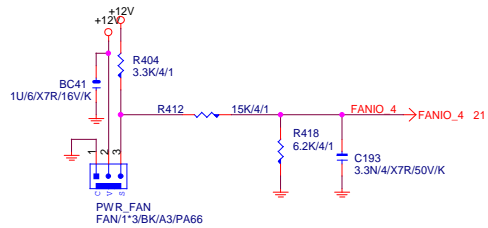
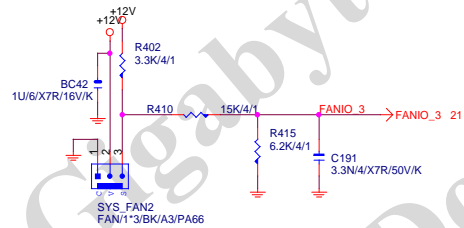
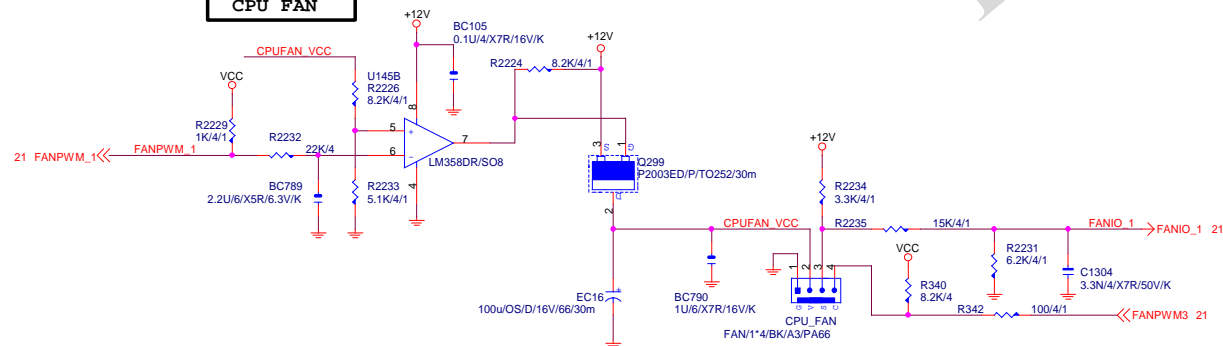
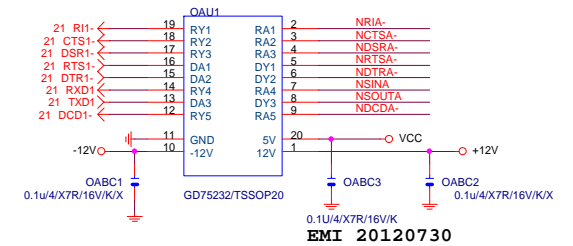


11NR6-403007-21R

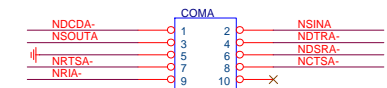
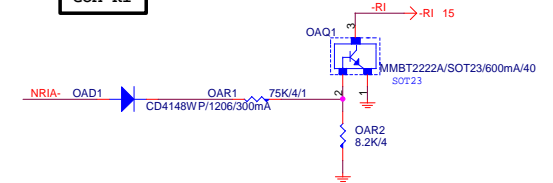
**LINE-OUT****LINE-IN****MIC-IN****SURROUND****CEN/LFE****SURRBACK****AZALIA FRONT PANEL**

Gigabyte Technology

Title		
AUDIO JACK		
Size Custom	Document Number	Rev
Date: Thursday, July 03, 2014	GA-990FXA-UD3	4.02
Sheet 24 of 35		

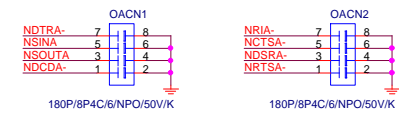
**SYSTEM FAN****POWER FAN****SYSTEM FAN2****CPU FAN****COMA**

EMI 20120730

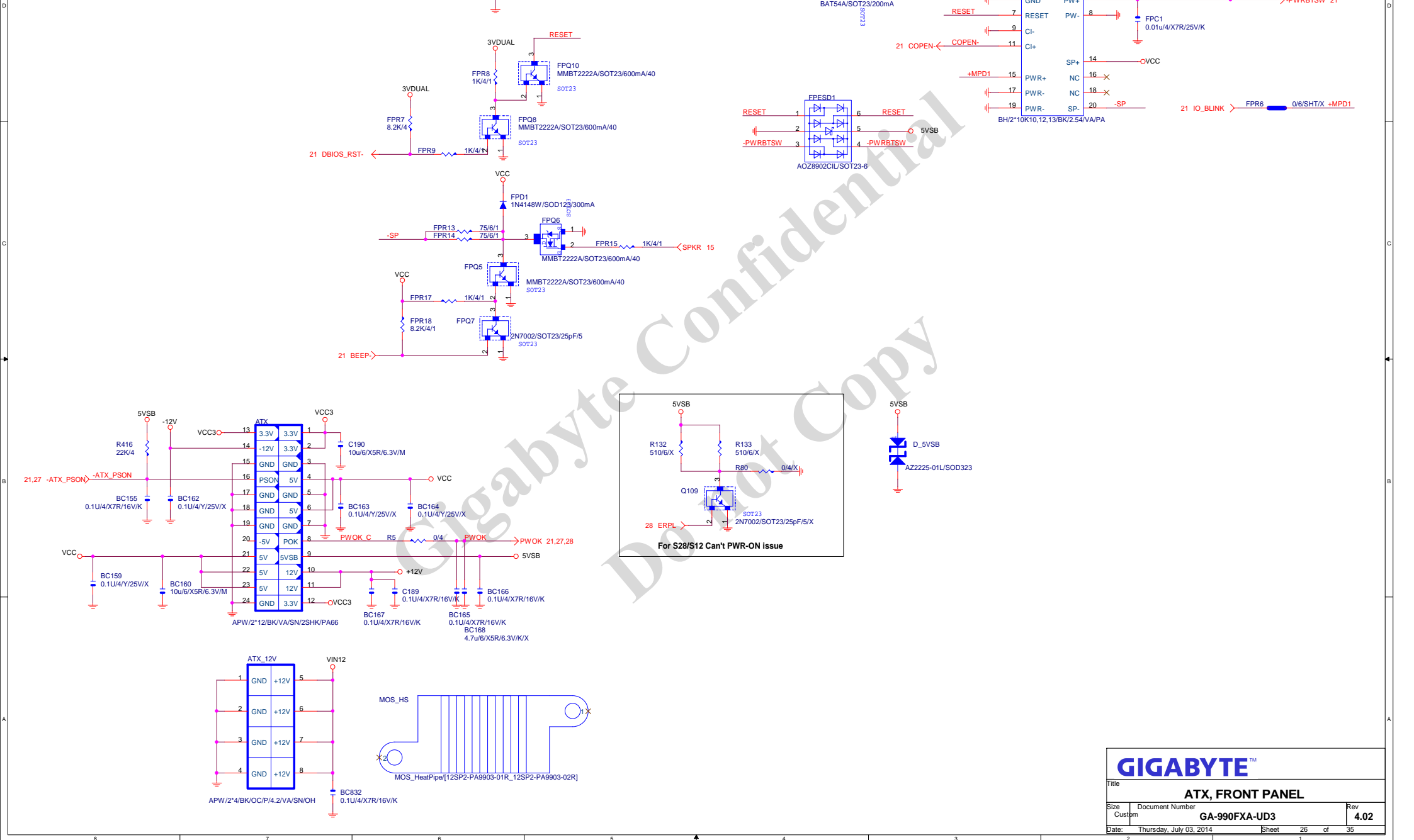
**COM RI**

BH2\*5K10/BK/2.54VVA/COM

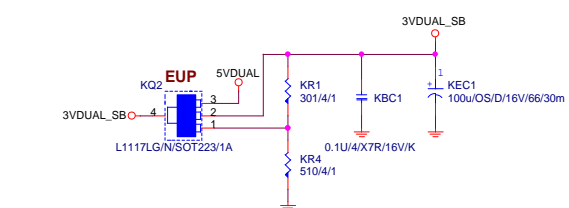
11NH3-000205-Y1R/Y2R

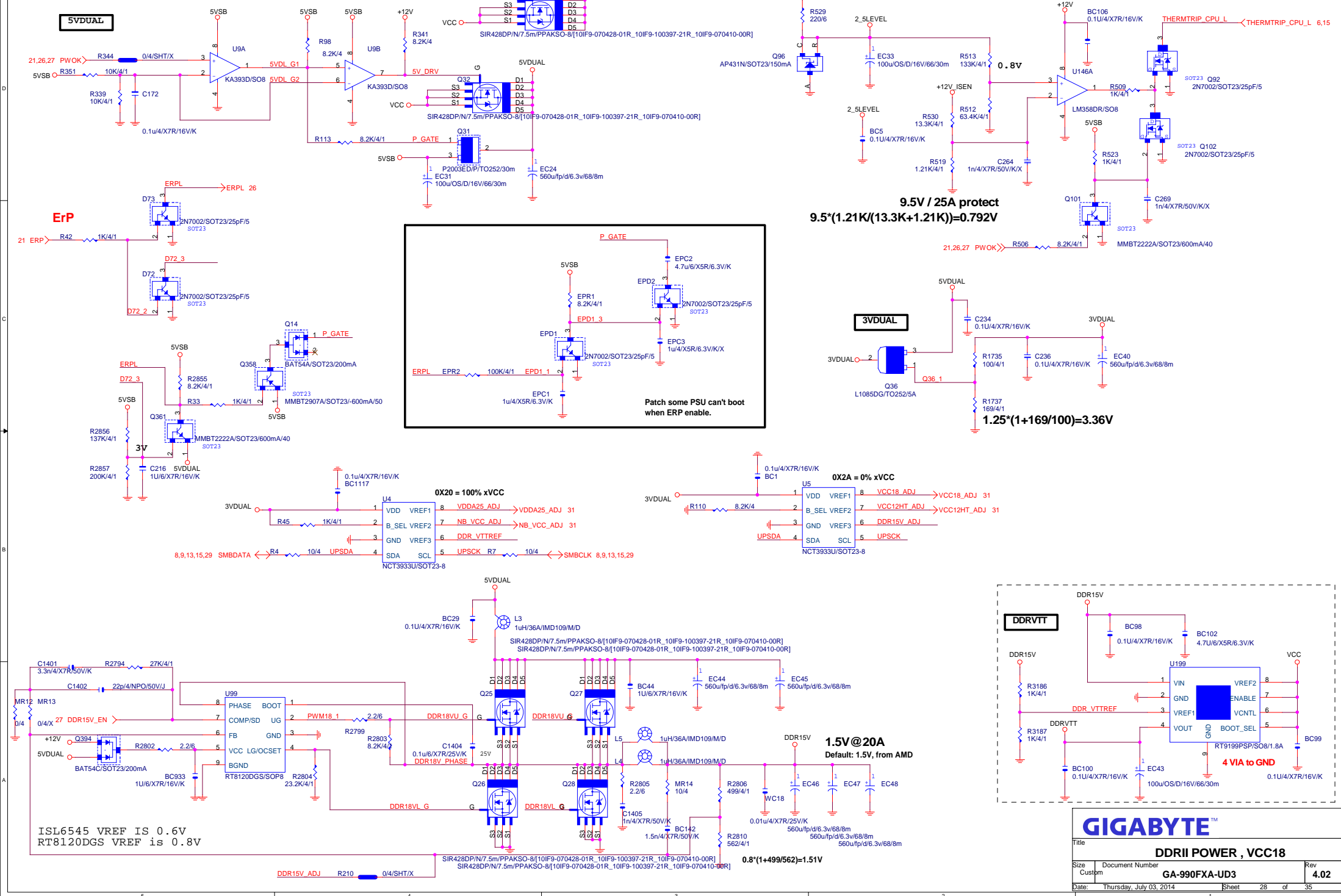
**GIGABYTE**

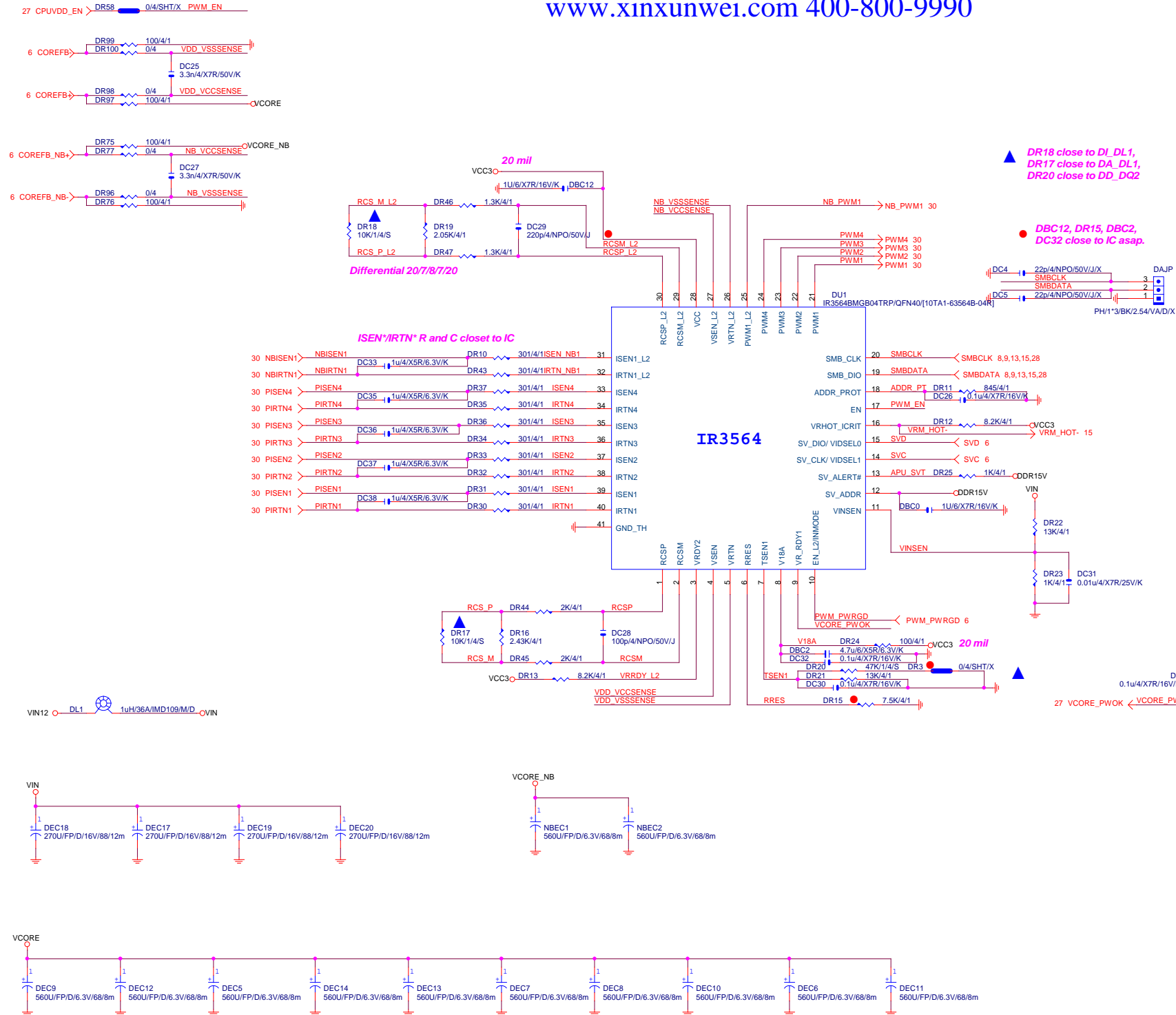
Title			FAN/HWMO/COM	
Size	Document Number	GA-990FXA-UD3		Rev
Custom				4.02
Date:	Thursday, July 03, 2014	Sheet	25	of 35







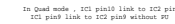
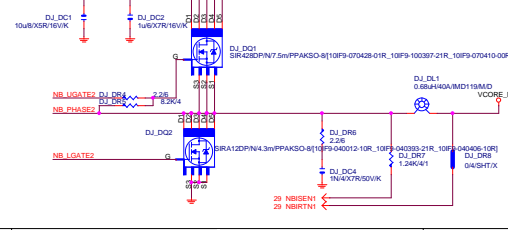
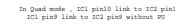


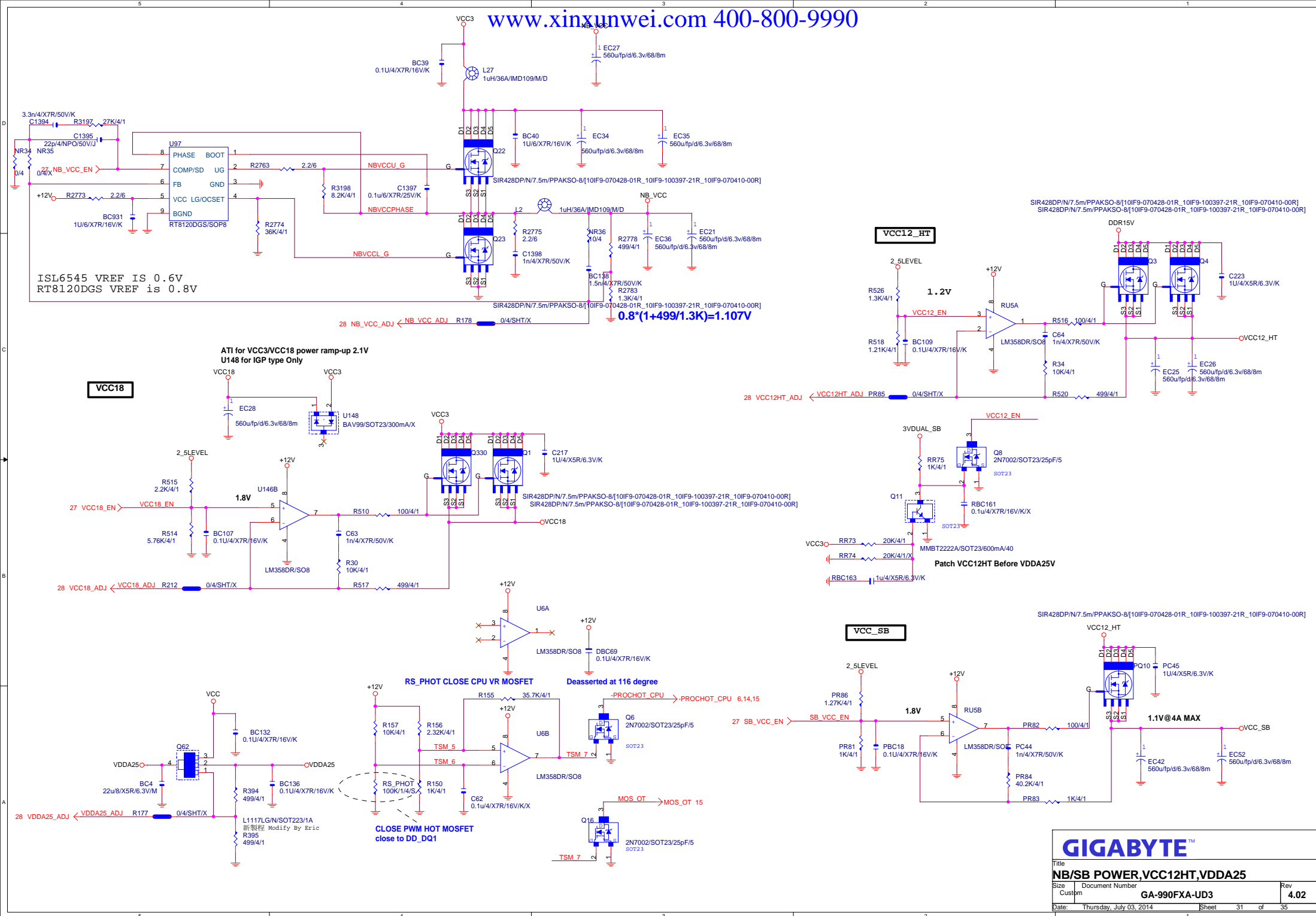


GIGABYTE™

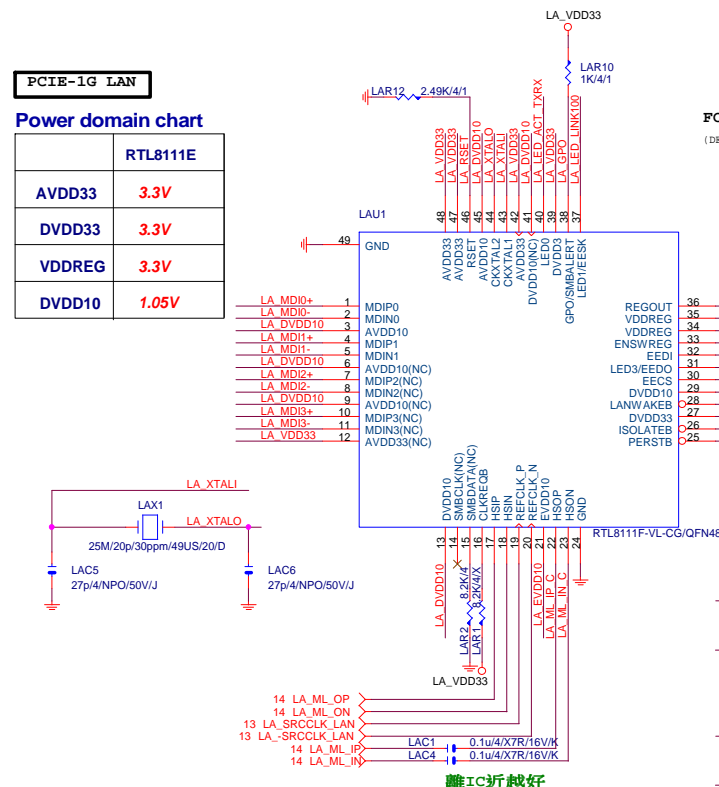
Title **Vcore (PWM IR3564+IR3598)**

Size	Document Number	Rev
Custom	<b>GA-990FXA-UD3</b>	<b>4.02</b>
Date:	Thursday, July 03, 2014	Sheet 29 of 35





	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

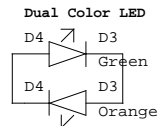


LA\_VDD33


LA ENSWREG

LAR8  
0/6/SHT/M/X

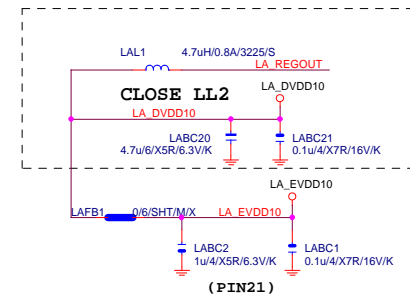
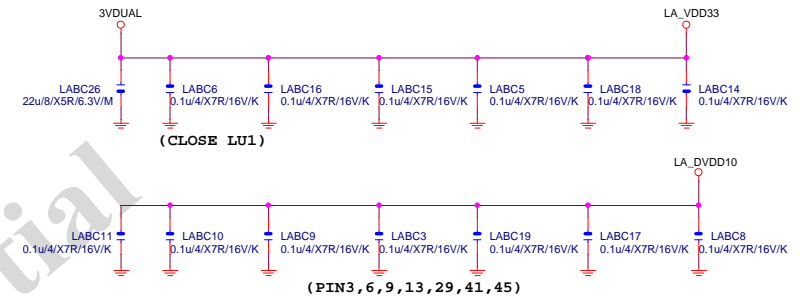
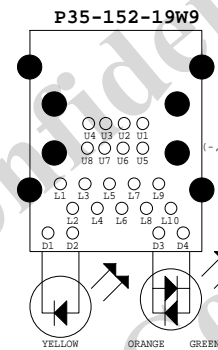
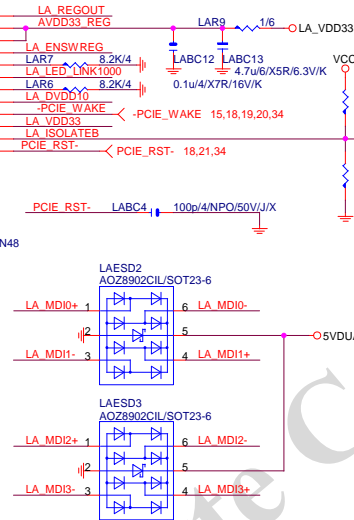
ENABLE SW



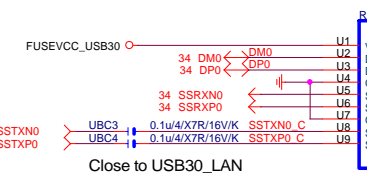
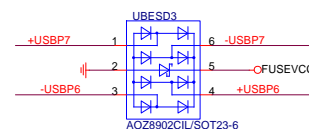
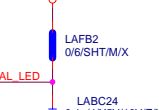
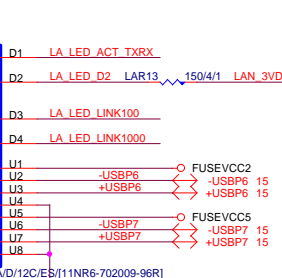
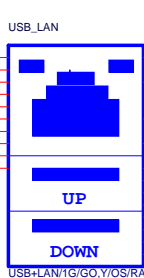
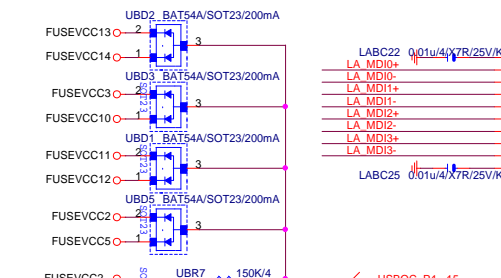
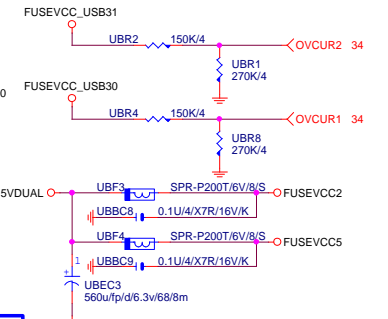
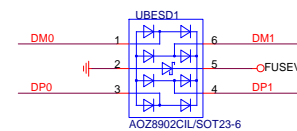
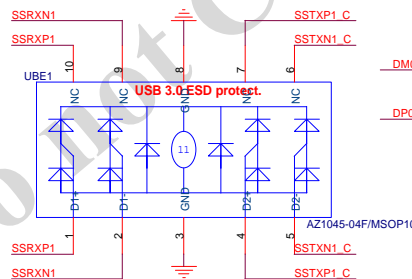
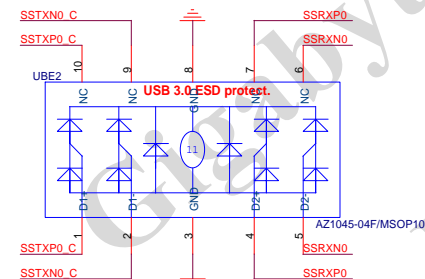
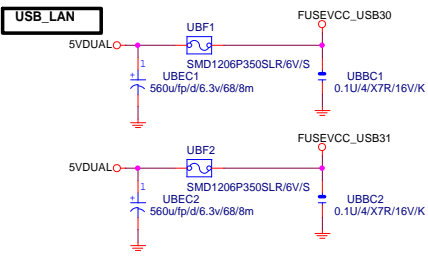
Single Color LED



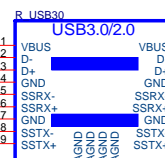
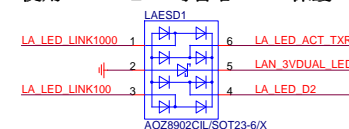
D2 D1  
Yellow



USB\_LAN



使用RU9 USB\_LAN可省略LAESD1保護LED



Close to USB30\_LAN  
90 欧姆: [20/4.5/7.5/4.5/20]

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Size	Document Number	Rev	
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Date:	Thursday, July 03, 2014	Sheet	32 of 35





